



Virtex 6 HXT x16PCIe Ethernet Solutions

HTG-V6HXT-x16PCIe Module

Mantaro HTG-V6HXT-x16PCIe is the first in class PCI Express Gen2 module to support x16 PCIe connectivity, thus, enabling 40Gbps throughput optical interface designs including 40Gbps Ethernet. This Mantaro module overcomes the inherent PCIe limitation of the current high end FPGA family from Xilinx, namely the Virtex-6 family.

The HTG-V6HXT-x16PCIe provides industry leading **64Gbps** PCIe. The HTG-V6HXT-x16PCIe module includes a x16 capable Gen2 PCIe switch between the edge connector and the FPGA. The PCIe switch provides a x16 Gen2 PCIe edge connection for the module and connects to two x8 Gen2 PCIe endpoints on the Virtex-6 FPGA. This extends the Virtex-6 which natively supports x8 Gen2 PCIe endpoints that have a maximum throughput of a single endpoint of 32Gbps (8 * 5Gbps * 0.8 [8B/10B coding efficiency]).

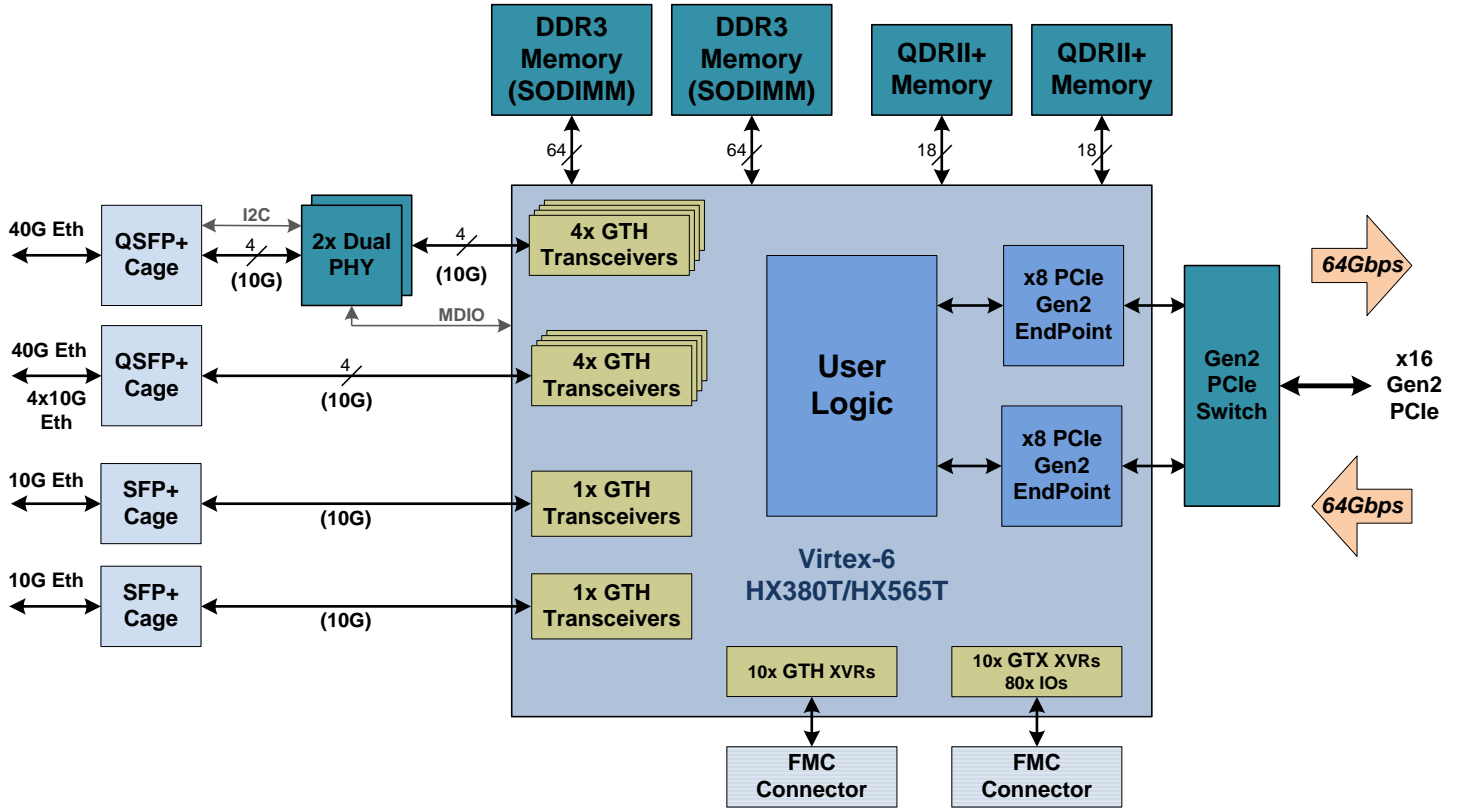
This innovation along with dual 64-bit DDR3 memories, Dual 18-bit QDRII+, and Dual 11.3Gbps QSFP+ interfaces enables 40Gbps throughput designs including 40Gbps IEEE802.3ba compliant Ethernet. HTG-V6HXT-x16PCIe can be used as a highly configurable/customizable 40Gbps NIC and 40Gbps network analyzer.

Additionally, ten 11.18Gbps/link capable HXT links on the FMC connector allows the HTG-V6HXT-x16PCIe module to be used as an evaluation platform for the 100Gbps Ethernet/OTN solutions.

Key features of the HTG-V6HXT-x16PCIe module are:

- Single Xilinx Virtex6 HX380T or HX565T FPGA
- x16 PCI Express Edge Connector (Gen2 PCIe)
- 1 QSFP+ port with EDC support through two external PHY chips and interface to the on-board FPGA's GTH (10G) serial transceivers
- 1 QSFP+ port with direct interface to the on-board FPGA's GTH (10G) serial transceivers
- 2 SFP+ ports with direct interface to the on-board FPGA's GTH (10G) serial transceivers
- 2 64-bit DDR-3 SODIMM (up to 16GB) memory
- 2 18-bit QDR-II+ memory
- 1 SMA Port (10G)
- 2 FMC Connectors
 - FMC #1: 40 LVDS IOs and 10 GTX (6.6 Gbps) Serial IOs
 - FMC # 2: 10 GTH (11.18 Gbps) Serial IOs
- Configuration through JTAG or CPLD
- USB to UART controller
- ATX and DC power supplies for PCI Express and stand alone operations

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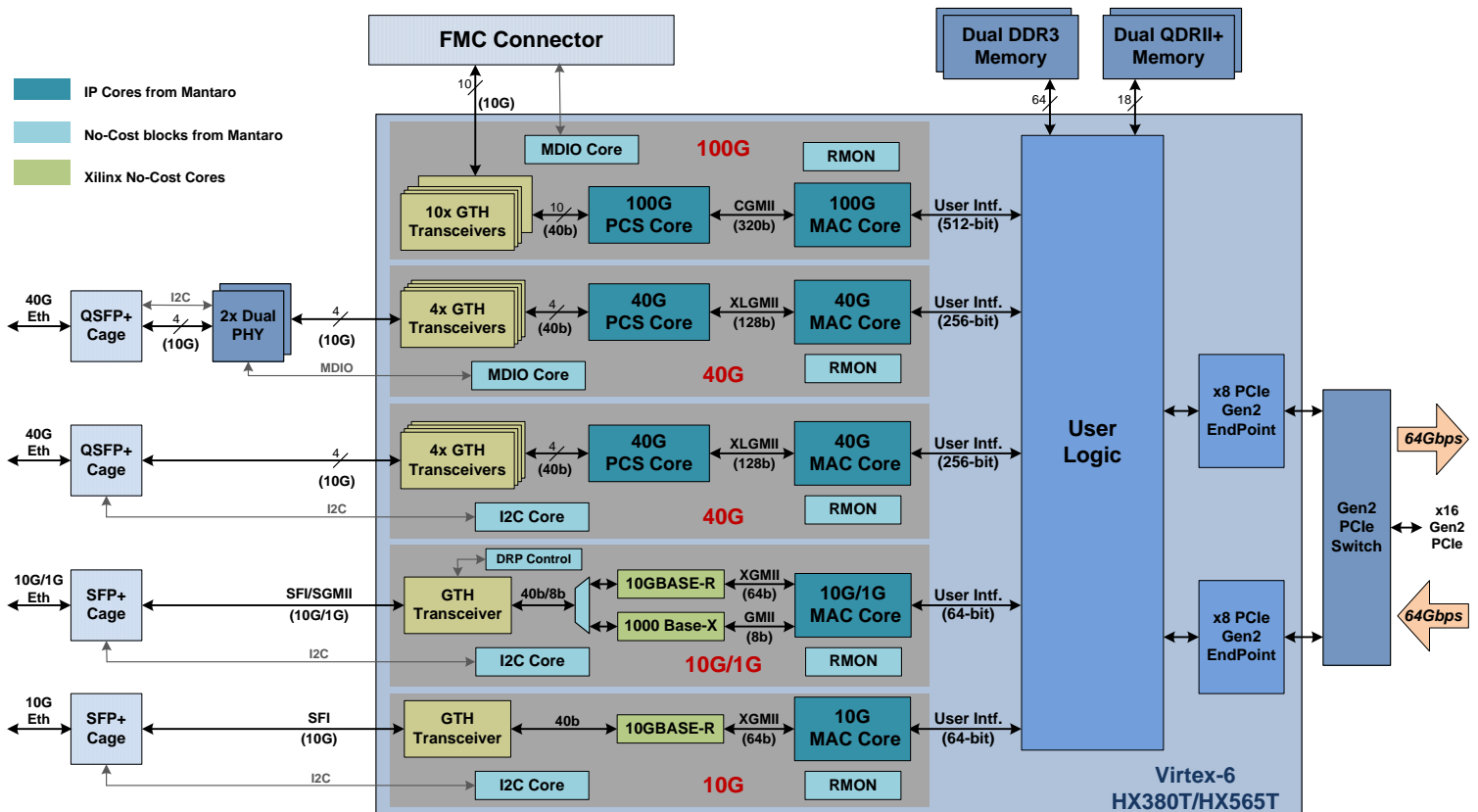
Ethernet IP Solutions for the HTG-V6HXT-x16PCIe Module

Dual QSFP+ and Dual SFP+ interfaces of the HTG-V6HXT-x16PCIe modules can be used to implement multi-port 40Gbps, 10Gbps and 1Gbps Ethernet solutions. Additionally, the FMC connector with 10 HXT transceivers interface can be used for evaluating the 100Gbps Ethernet solution. Ethernet IP solutions provided by Mantaro for the HTG-V6HXT-x16PCIe module are:

- **100Gbps** 802.3ba Compliant Ethernet; Based upon Mantaro supplied 100G MAC and 100G PCS IP cores; 10x 10Gbps links on the FMC connector
- **40Gbps** 802.3ba Compliant Ethernet; Based upon Mantaro supplied 40G MAC and 40G PCS IP cores; 4x 10Gbps links on the QSFP+ cages
- **10Gbps/1Gbps** 802.3-2008 compliant, runtime configurable 10Gbps/1Gbps dual-mode Ethernet; Based upon Mantaro supplied 10G/1G MAC core and Xilinx no-charge 10GBASE-R plus 1000Base-X PCS cores; 1x 10Gbps link on the SFP+ cages
- **10Gbps only** 802.3-2008 compliant Ethernet; Based upon Mantaro supplied 10G MAC core and Xilinx no-charge core; 1x 10Gbps link on the SFP+ cages

All Ethernet solutions are supplied with no-charge statistics (RMON) block. If required, MDIO, I2C and DRP Controller cores to control and configure the external PHYs/XVRs and GTH blocks are also provided by Mantaro on a no-charge basis as part of the Ethernet solution.

Following diagram shows the module elements and the IP blocks used for the Ethernet solutions:





Virtex 6 HXT x16PCIe Ethernet Solutions

40G/100G MAC Core Summary

- Highly optimized 320-bit data path design at 312.5MHz for 100Gbps mode
- 512-bit user interface @ 312.5MHz (non-segmented) or 512-bit user interface @ 225MHz (segmented) for 100Gbps mode
- 320-bit data path and 512-bit user interface (non-segmented) @ 125MHz for 40Gbps mode

Device	RMON	Slices	Slice LUTS	Slice Registers	Memory 18k/36k BRAM
VIRTEX6 - 2C	Yes	6,854	18,098	19,866	4 – 18k BRAM 14 – 36k BRAM
	No	5,960	16,398	18,035	4 – 18k BRAM 14 – 36k BRAM

100G PCS Core Summary

- Highly optimized 320-bit data path design at 312.5MHz
- 10x 10.3125Gbps links for 10x 10G interface to the CFP module or 10x 10G interface to Fiber links

Device	Slices	Slice LUTs	Slice Registers	Memory 18k/36k BRAM
VIRTEX6 - 2C	10,780	27,164	33,335	0 – 18k BRAM 60 – 36k BRAM

40G MAC Core Summary

- Highly optimized 128-bit data path design at 312.5MHz
- Flexible 128-bit @ 312.5MHz or 256-bit @ 225MHz user interfaces

Device	User Interface Width	RMON and MDIO	Slices	Slice LUTS	Slice Registers	Memory 18k/36k BRAM
VIRTEX6 - 2C	128-Bit	Yes	2,605	6,415	7,629	3 – 18k BRAM 8 – 36k BRAM
		No	2,605	4,769	5,909	3 – 18k BRAM 8 – 36k BRAM
	256-Bit	Yes	2,877	7,102	9,099	3 – 18k BRAM 12 – 36k BRAM
		No	2,292	5,473	7,379	3 – 18k BRAM 12 – 36k BRAM



Virtex 6 HXT x16PCIe Ethernet Solutions

40G PCS Core Summary

- Highly optimized 128-bit data path design at 312.5MHz
- 4x 10.3125Gbps links for 4x10G fiber interface (through QSFP+ plug-in transceivers)

Device	Slices	Slice LUTs	Slice Registers	Memory 18k/36k BRAM
VIRTEX6 – 2C	3,230	8,452	10,159	1 – 18k BRAM 24 – 36k BRAM

10G/1G MAC Core Summary

- 64-bit data path design at 156.25MHz
- 64-bit user (application layer) interface
- Run-time configurable selection of 10Gbps and 1Gbps mode of operation
- Provides the flexibility to switch between 1G and 10G operation based upon the type of SFP (optical/electrical) transceiver plugged into the SFP cage without separate image downloads
- Provides RJ-45 GiGE Ethernet interface for the HTG-V6HXT-x16PCIe through 1000-BaseX copper SFP plug-in module

Device	RMON and MDIO	Slices	Slice LUTS	Slice Registers	Memory 18k/36k BRAM
VIRTEX6 – 2C	Yes	2,251	6,537	5,805	1 – 18k BRAM 6 – 36k BRAM
	No	1,784	4,662	4,745	1 – 18k BRAM 6 – 36k BRAM

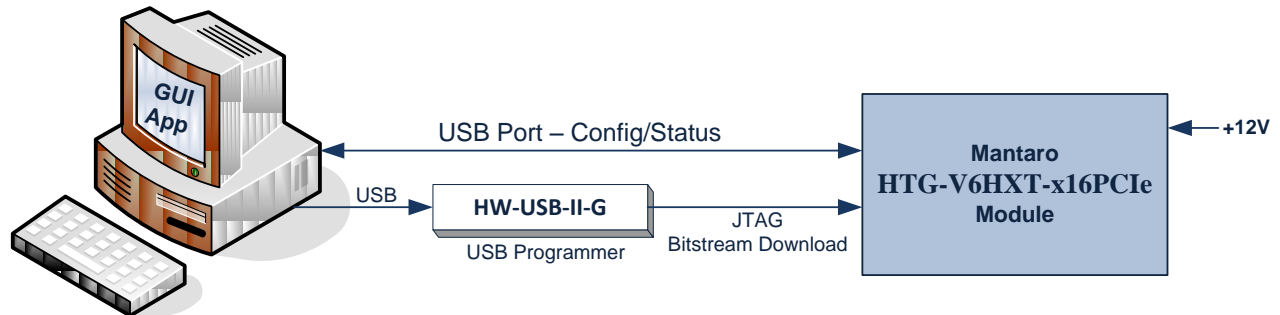
10G MAC Core Summary

- 64-bit data path design at 156.25MHz
- 64-bit user (application layer) interface

Device	RMON and MDIO	Slices	Slice LUTS	Slice Registers	Memory 18k/36k BRAM
VIRTEX6 – 2C	Yes	2,167	6,144	5,344	1 – 18k BRAM 6 – 36k BRAM
	No	1,773	4,313	4,280	1 – 18k BRAM 6 – 36k BRAM

Demonstration/Evaluation Setup for Mantaro Ethernet Solutions

As shown in the figure below, Ethernet demonstration and core evaluation setup uses a Windows PC running a custom GUI application to configure and control the HTG-V6HXT-x16PCIe module. The module is powered in stand-alone mode of operation and a Xilinx USB programmer is used to load the FPGAs images. Another USB interface to the module (through the USB-UART converter) is used to configure, control and gather statistics from the FPGA on the HTG-V6HXT-x16PCIe module.

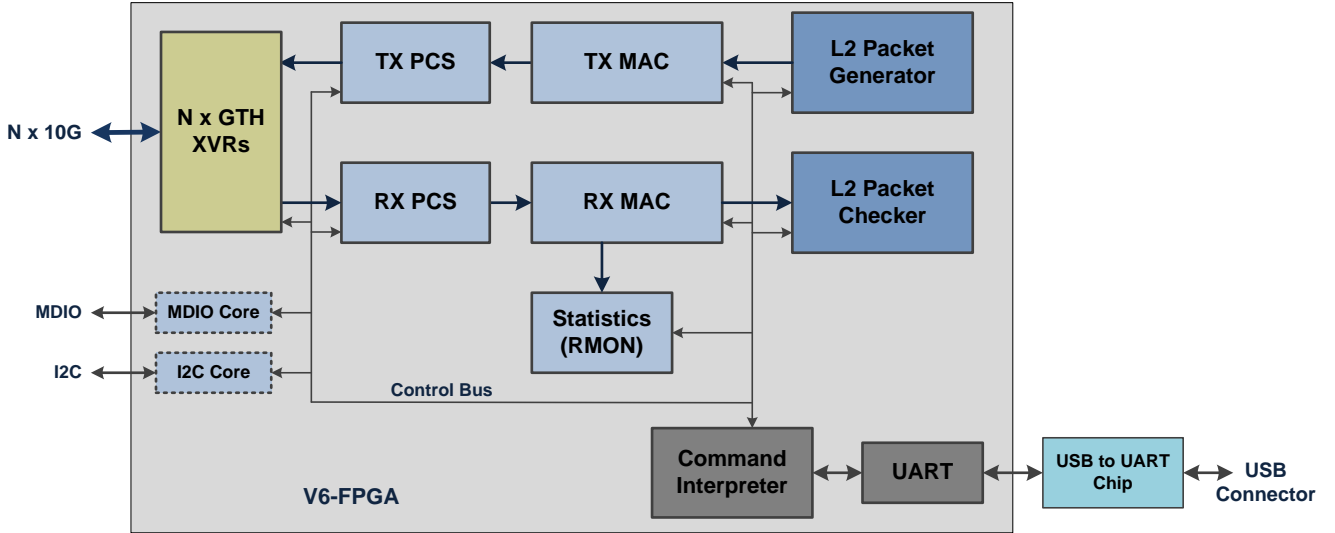


Five Ethernet demonstration and evaluation setups are provided by Mantaro for the HTG-V6HXT-x16PCIe module. These five setups exercise five high speed physical interfaces available on the module. The five setups for the HTG-V6HXT-x16PCIe module are:

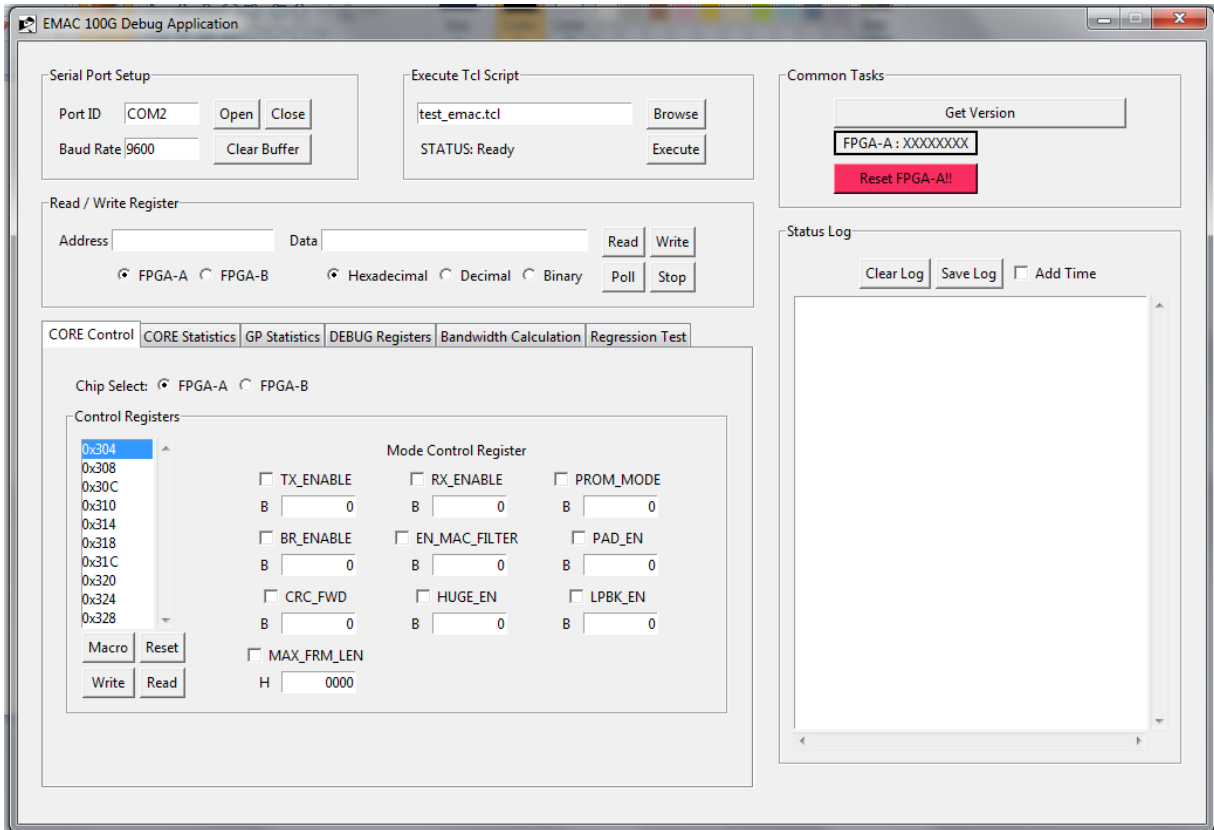
1. **100Gbps** Ethernet evaluation setup using 10 GTH transceivers that are routed to the FMC connector.
2. **40Gbps** Ethernet setup through 4 GTH transceivers that are connected to the two external dual-transceiver PHY devices. The outputs/inputs of the PHY device then connect to the QSFP+ cage. Demo application implements the configuration and control of the two external PHYs through the MDIO control interface.
3. **40Gbps** Ethernet setup through 4 GTH transceivers that are connected directly to the QSFP+ cage
4. **10G/1G** Ethernet setup using 1 GTH transceiver that is connected directly to the first SFP+ cage. Demo application for this setup implements the I2C interface to the SFP module to identify the type of the module inserted in the cage (10G or 1G). A DRP controller is also implemented to dynamically configure the GTH transceiver and PLLs for 10G or 1G mode of operation.
5. **10G** only Ethernet setup using 1 GTH transceiver that is connected directly to the second SFP+ cage.

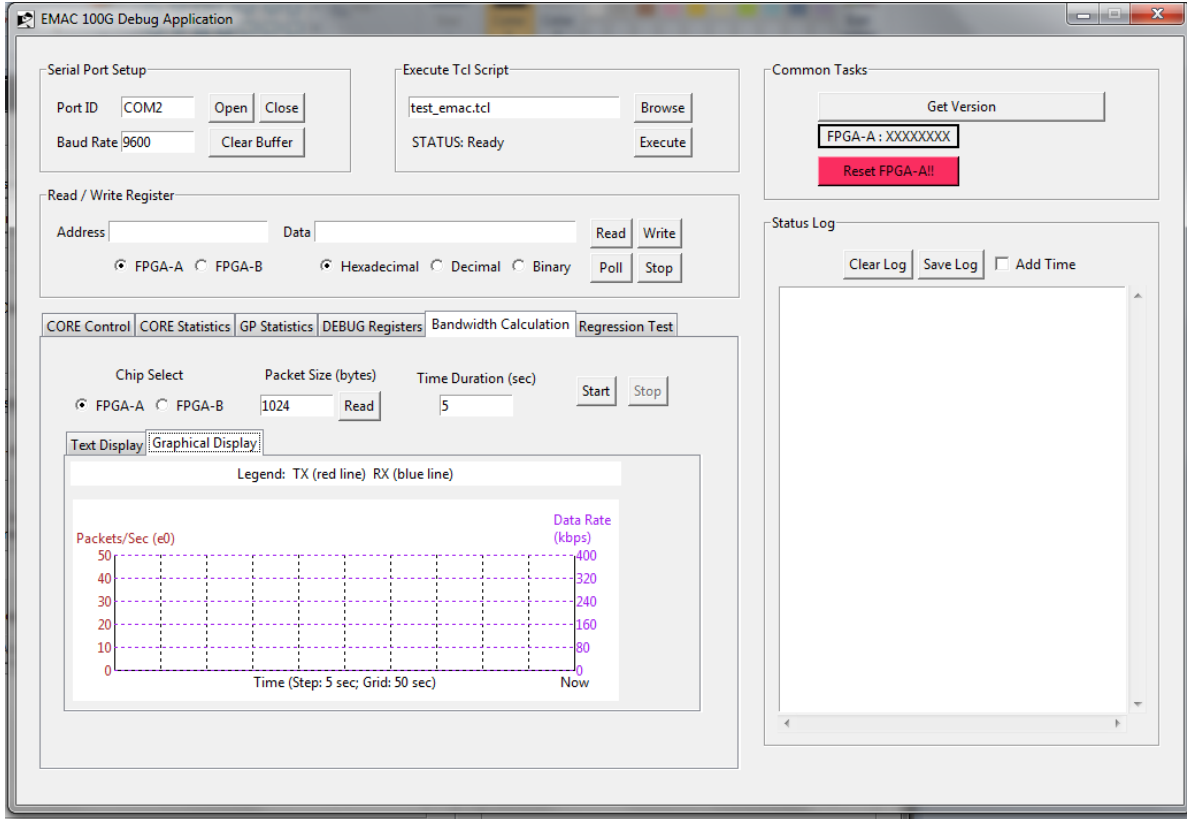
Each of the demonstration and evaluation setups uses a line speed (up to 100Gbps) L2 Ethernet packet generator and checker along with the Ethernet (MAC/PCS) and interface cores required for each setup. The following is a generic block diagram for all evaluation and demonstration setups.

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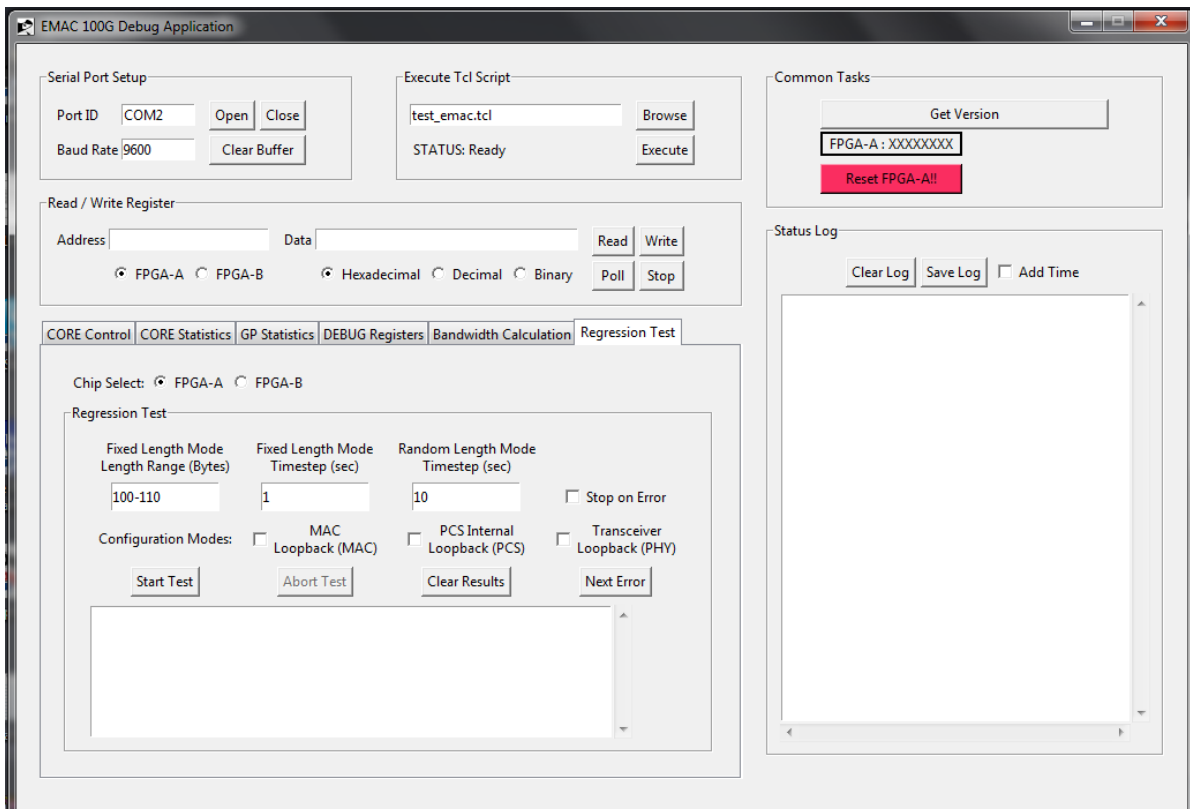


Following snap-shots shows the interface of the GUI application running on the PC.





The screenshot shows the 'EMAC 100G Debug Application' interface. The 'Regression Test' tab is active, displaying a graphical display of network performance metrics. The graph plots 'Packets/Sec (e0)' on the left y-axis (0 to 50) and 'Data Rate (kbps)' on the right y-axis (0 to 400) against 'Time (Step: 5 sec; Grid: 50 sec)' on the x-axis. A legend indicates TX (red line) and RX (blue line). The graph shows a steady increase in both metrics over time, with TX reaching approximately 45 packets/sec and Data Rate reaching approximately 360 kbps.



The screenshot shows the 'EMAC 100G Debug Application' interface with the 'Regression Test' configuration options. The 'Chip Select' is set to 'FPGA-A'. The 'Regression Test' section includes the following settings:

- Fixed Length Mode Length Range (Bytes): 100-110
- Fixed Length Mode Timestep (sec): 1
- Random Length Mode Timestep (sec): 10
- Stop on Error:
- Configuration Modes:
 - MAC Loopback (MAC):
 - PCS Internal Loopback (PCS):
 - Transceiver Loopback (PHY):

Buttons for 'Start Test', 'Abort Test', 'Clear Results', and 'Next Error' are visible at the bottom of the configuration section.