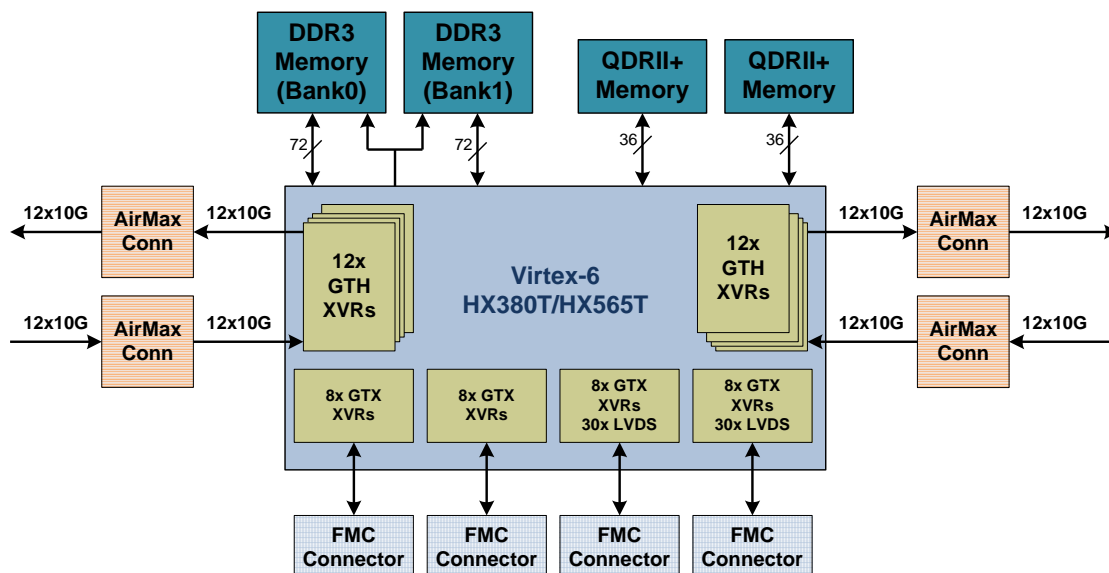


### HTG-V6HXT-100G Module

Mantaro HTG-V6HXT-100G module is designed as an evaluation platform for 100Gbps networking and communication protocols including 100Gbps Ethernet, OTN and 100Gbps Interlaken. Integration of highest density Virtex-6 FPGA with DDR3 and QDRII+ memories, two 120Gbps Interlaken interfaces (12x10Gbps lanes with FCI AirMax connectors) on two edges of the module, 4 FMC interfaces and available extender modules makes HTG-V6HXT-100G a versatile development platform.

Key features of the HTG-V6HXT-100G module:

- One Xilinx Virtex-6 HX380T or HX565T-2FFG1923 FPGA
- 144-bit dual-bank (72x2) DDR3 memory using 10 Micron MT41J64M16LA-15E devices
- Two 36-bit QDRII+ memories using 4 Cypress CY7C2563KV18 (72-Mbit each) devices
- 4 FMC (FPGA Mezzanine Card, Vita 57) Connectors
  - Connector #1: 8 GTX serial transceivers, 66 single-ended IOs (33LVDS), Clocks, JTAG, and PWR.
  - Connector #2: 8 GTX serial transceivers, 66 single-ended IOs (33LVDS), Clocks, JTAG, and PWR.
  - Connector #3: 8 GTX serial transceivers, Clocks, JTAG, and PWR.
  - Connector #4: 8 GTX serial transceivers, Clocks, JTAG, and PWR.
- Samtec QSE Connectors with 8 additional GTX serial transceivers
- Two Interlaken interfaces on each edge of the module with:
  - 12 transmit and receive lanes (@11.3 Gbps) with robust CEI electrical performance
  - Up to 100G of Interlaken bandwidth
  - FCI AirMax Connector for interoperability with existing line cards
- Legacy module interfaces including SFP+, XFP and emerging interfaces such as CFP and CXP using FMC and AirMax compatible extender modules
- USB 2.0 Host and Device / UART
- Programmable Clock Generators & Synthesizers



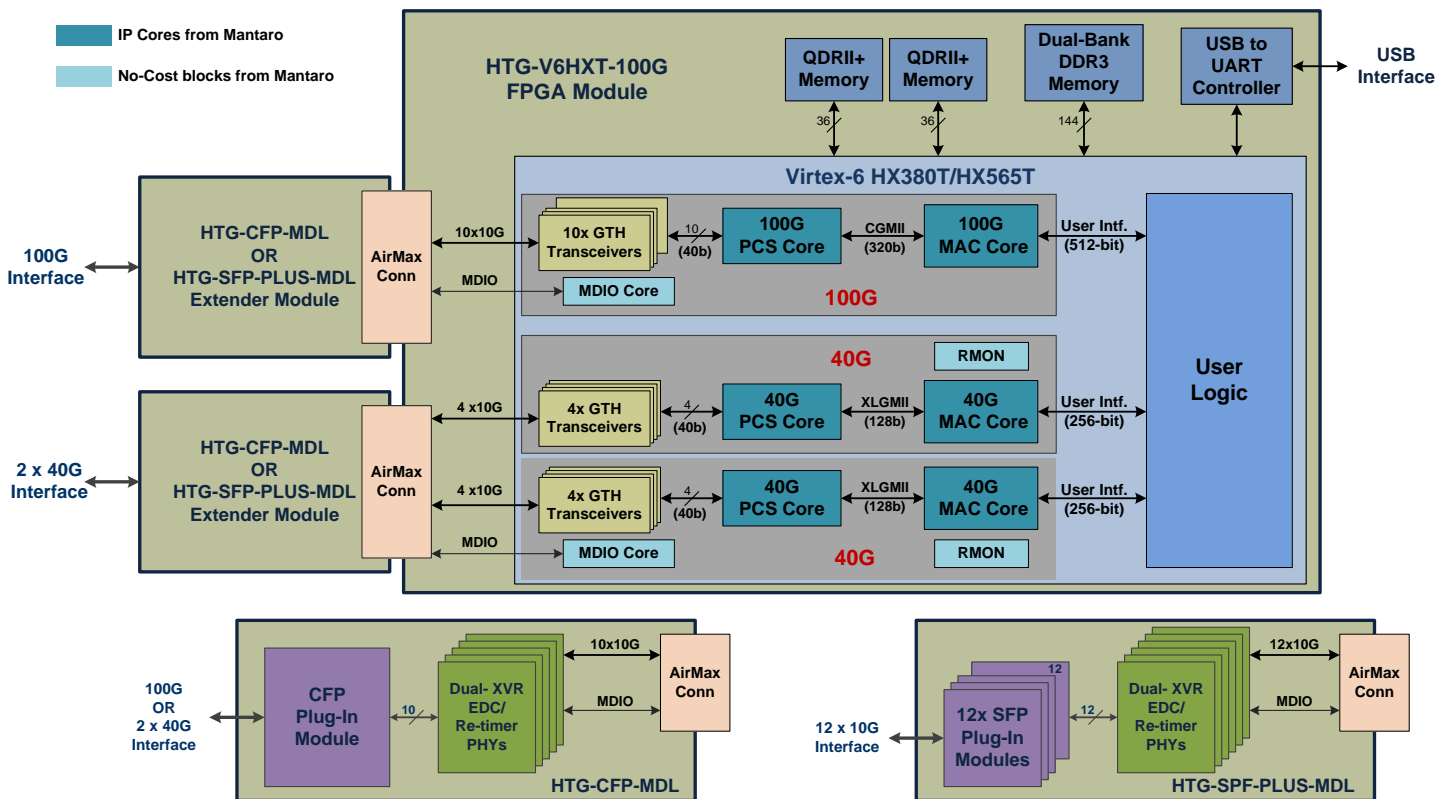
## Ethernet IP Solutions for the HTG-V6HXT-100G Module

HTG-V6HXT-100G module can be used as an evaluation platform for 100Gbps, 40Gbps 10Gbps and 1Gbps Ethernet solutions by connecting the module to various AirMax extender modules (available from Mantaro). Ethernet IP solutions provided by Mantaro for the module are:

- **100Gbps** 802.3ba Compliant Ethernet; Based upon Mantaro supplied 100G MAC and 100G PCS IP cores; 10x 10Gbps links on the AirMax connector to CFP/SFP+ extender module
- **40Gbps** 802.3ba Compliant Ethernet; Based upon Mantaro supplied 40G MAC and 40G PCS IP cores; 4x 10Gbps links on the AirMax connector to CFP/SFP+ extender module
- **10Gbps/1Gbps** 802.3-2008 compliant, runtime configurable 10Gbps/1Gbps dual-mode Ethernet; Based upon Mantaro supplied 10G/1G MAC core and Xilinx no-charge 10GBASE-R plus 1000Base-X PCS cores; 1x 10Gbps link on the AirMax connector to SFP+ extender module
- **10Gbps only** 802.3-2008 compliant Ethernet; Based upon Mantaro supplied 10G MAC core and Xilinx no-charge core; 1x 10Gbps link on the AirMax connector to SFP+ module

All Ethernet solutions are supplied with no-charge statistics (RMON) block. If required, MDIO, I2C and DRP Controller cores to control and configure the external PHYs/XVRs and GTH blocks are also provided by Mantaro on a no-charge basis as part of the Ethernet solution.

Following diagram shows the elements and the IP blocks used for the 100G and Dual 40G Ethernet solutions for the HTG-V6HXT-100G module mated with either the HTG-CFP-MDL or HTG-SPF-PLUS-MDL AirMax extender modules:





## Virtex 6 HXT 100G Ethernet Solutions

### 40G/100G MAC Core Summary

- Highly optimized 320-bit data path design at 312.5MHz for 100Gbps mode
- 512-bit user interface @ 312.5MHz (non-segmented) or 512-bit user interface @ 225MHz (segmented) for 100Gbps mode
- 320-bit data path and 512-bit user interface (non-segmented) @ 125MHz for 40Gbps mode

<b>Device</b>	<b>RMON</b>	<b>Slices</b>	<b>Slice LUTS</b>	<b>Slice Registers</b>	<b>Memory 18k/36k BRAM</b>
VIRTEX6 - 2C	Yes	6,854	18,098	19,866	4 – 18k BRAM 14 – 36k BRAM
	No	5,960	16,398	18,035	4 – 18k BRAM 14 – 36k BRAM

### 100G PCS Core Summary

- Highly optimized 320-bit data path design at 312.5MHz
- 10x 10.3125Gbps links for 10x 10G interface to the 100Gbps CFP on HTG-CFP-MDL extender module or 10x 10G SFP+ interfaces on HTG-SPF-PLUS-MDL extender module

<b>Device</b>	<b>Slices</b>	<b>Slice LUTs</b>	<b>Slice Registers</b>	<b>Memory 18k/36k BRAM</b>
VIRTEX6 - 2C	10,780	27,164	33,335	0 – 18k BRAM 60 – 36k BRAM

### 40G MAC Core Summary

- Highly optimized 128-bit data path design at 312.5MHz
- Flexible 128-bit @ 312.5MHz or 256-bit @ 225MHz user interfaces

<b>Device</b>	<b>User Interface Width</b>	<b>RMON and MDIO</b>	<b>Slices</b>	<b>Slice LUTS</b>	<b>Slice Registers</b>	<b>Memory 18k/36k BRAM</b>
VIRTEX6 - 2C	128-Bit	Yes	2,605	6,415	7,629	3 – 18k BRAM 8 – 36k BRAM
		No	2,605	4,769	5,909	3 – 18k BRAM 8 – 36k BRAM
	256-Bit	Yes	2,877	7,102	9,099	3 – 18k BRAM 12 – 36k BRAM
		No	2,292	5,473	7,379	3 – 18k BRAM 12 – 36k BRAM



## Virtex 6 HXT 100G Ethernet Solutions

### 40G PCS Core Summary

- Highly optimized 128-bit data path design at 312.5MHz
- 4x 10.3125Gbps links for 4x10G fiber interface to the dual 40G CFP to the CFP on HTG-CFP-MDL extender module or 4x 10G SFP+ interfaces on HTG-SPF-PLUS-MDL extender module

<b>Device</b>	<b>Slices</b>	<b>Slice LUTs</b>	<b>Slice Registers</b>	<b>Memory 18k/36k BRAM</b>
VIRTEX6 – 2C	3,230	8,452	10,159	1 – 18k BRAM 24 – 36k BRAM

### 10G/1G MAC Core Summary

- 64-bit data path design at 156.25MHz
- 64-bit user (application layer) interface
- Run-time configurable selection of 10Gbps and 1Gbps mode of operation
- Provides the flexibility to switch between 1G and 10G operation based upon the type of SFP (optical/electrical) transceiver plugged into the SFP cage without separate image downloads
- Provides RJ-45 GiGE Ethernet interface for the HTG-V6HXT-100G through 1000-BaseX copper SFP plugged into the HTG-SPF-PLUS-MDL extender module

<b>Device</b>	<b>RMON and MDIO</b>	<b>Slices</b>	<b>Slice LUTS</b>	<b>Slice Registers</b>	<b>Memory 18k/36k BRAM</b>
VIRTEX6 – 2C	Yes	2,251	6,537	5,805	1 – 18k BRAM 6 – 36k BRAM
	No	1,784	4,662	4,745	1 – 18k BRAM 6 – 36k BRAM

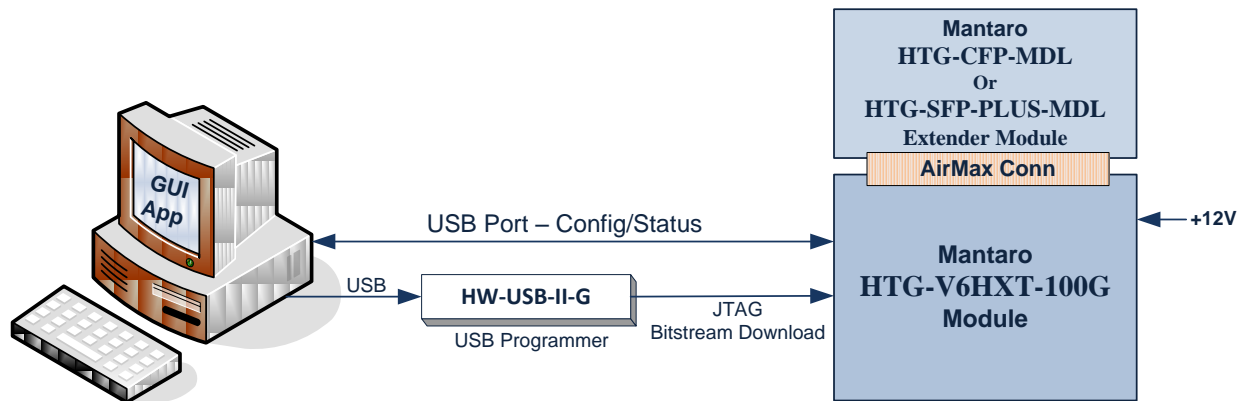
### 10G MAC Core Summary

- 64-bit data path design at 156.25MHz
- 64-bit user (application layer) interface

<b>Device</b>	<b>RMON and MDIO</b>	<b>Slices</b>	<b>Slice LUTS</b>	<b>Slice Registers</b>	<b>Memory 18k/36k BRAM</b>
VIRTEX6 – 2C	Yes	2,167	6,144	5,344	1 – 18k BRAM 6 – 36k BRAM
	No	1,773	4,313	4,280	1 – 18k BRAM 6 – 36k BRAM

### Demonstration/Evaluation Setup for Mantaro Ethernet Solutions

As shown in the figure below, Ethernet demonstration and core evaluation setup uses a Windows PC running a custom GUI application to configure and control the HTG-V6HXT-100G FPGA and HTG-CFP-MDL/HTG-SFP-PLUS-MDL extender modules. Modules are powered in stand-alone mode of operation and a Xilinx USB programmer is used to load the FPGAs images. Another USB interface to the module (through the USB-UART converter) is used to configure and control the FPGA and extender modules. It is also used to gather statistics from the FPGA on the HTG-V6HXT-100G module.

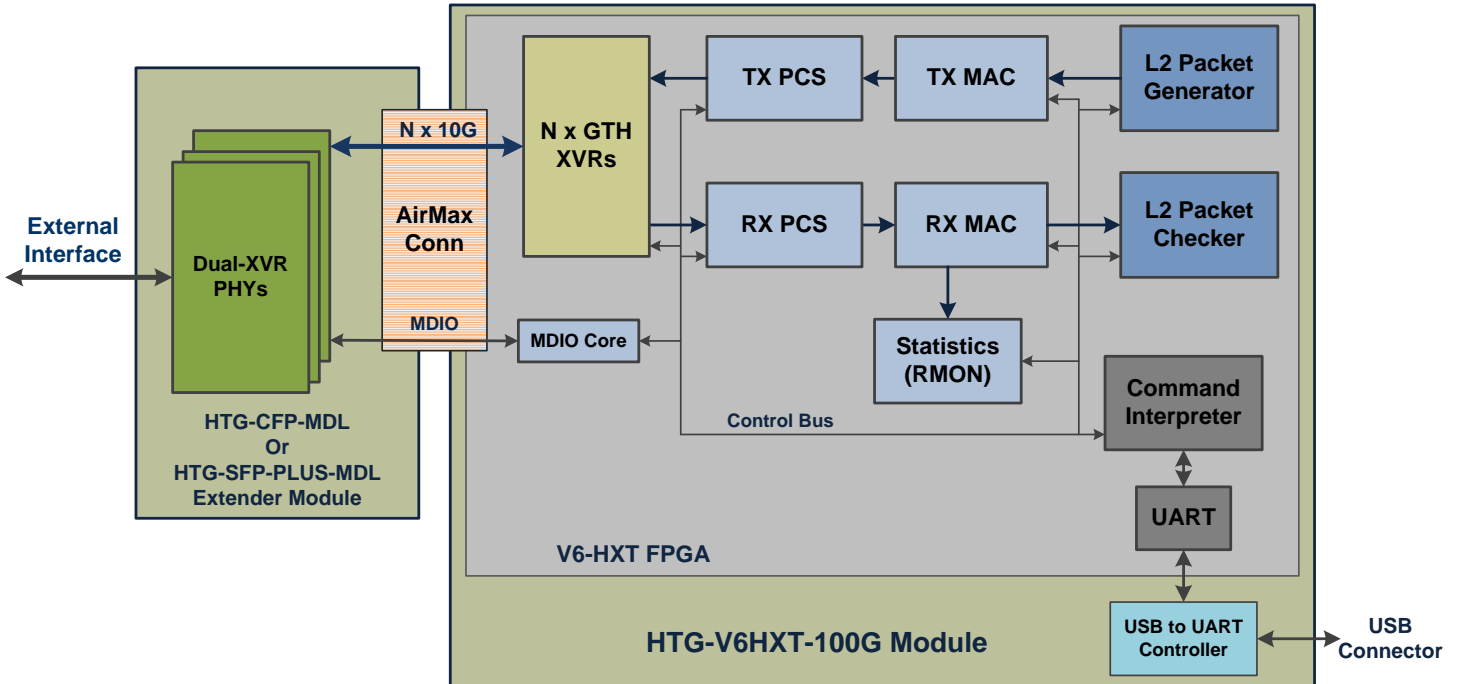


Four Ethernet demonstration and evaluation setups are provided by Mantaro for the HTG-V6HXT-100G module. All the evaluation setups implement the control and configuration of the extender modules. The four setups for the HTG-V6HXT-100G module are:

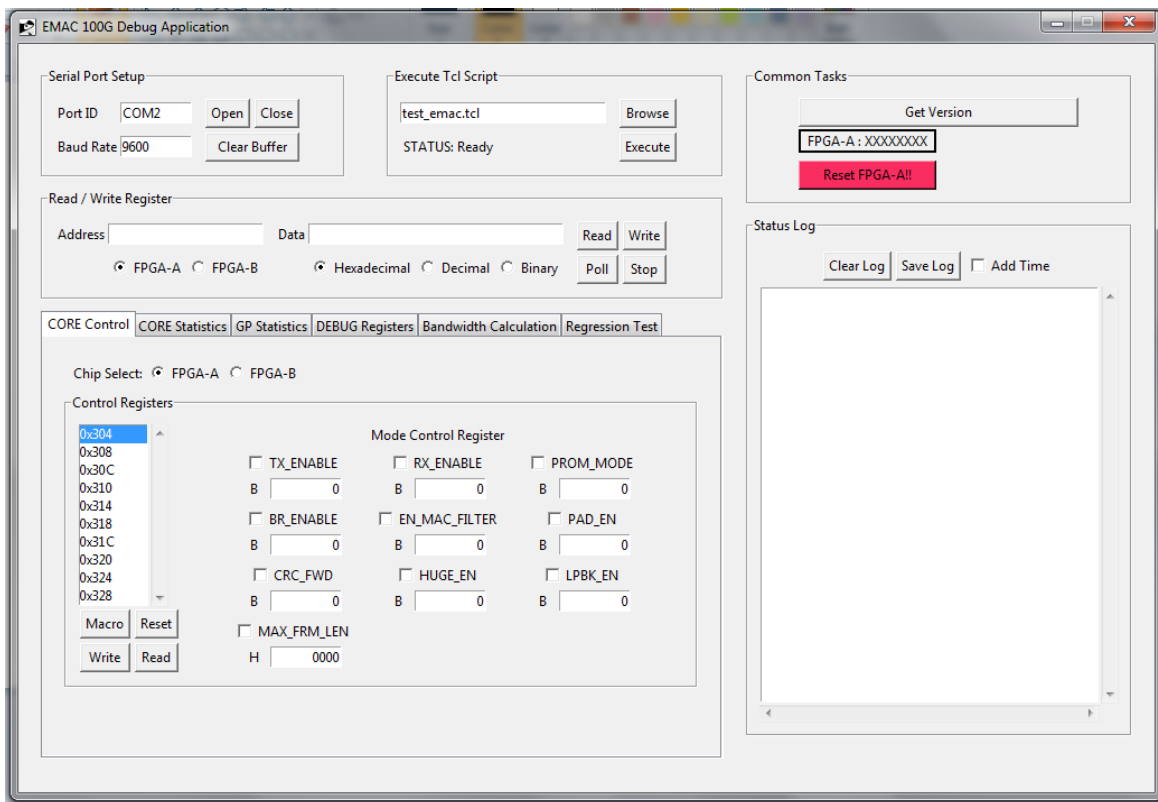
1. **100Gbps** Ethernet evaluation setup using the HTG-V6HXT-100G mated with HTG-CFP-MDL or HTG-SFP-PLUS-MDL extender modules. For the 100G demo using the HTG-CFP-MDL extender module, a 100Gbps CFP module is plugged into the CFP cage. When using HTG-SFP-PLUS-MDL extender module, 10 10Gbps SPF modules are plugged into the SFP+ cages.
2. **Dual 40Gbps** Ethernet evaluation setup using the HTG-V6HXT-100G mated with HTG-CFP-MDL or HTG-SFP-PLUS-MDL extender modules. For the dual 40G demo using the HTG-CFP-MDL extender module, a dual 40G CFP module is plugged into the CFP cage. When using HTG-SFP-PLUS-MDL extender module, 8 10Gbps SPF modules are plugged into the SFP+ cages.
3. **10G/1G** Ethernet evaluation setup using the HTG-V6HXT-100G mated with HTG-SFP-PLUS-MDL extender module with one SPF module plugged into the first SFP+ cage. Demo application for this setup implements the I2C interface to the SFP module (through the dual-PHY chip on the extender module) to identify the type of the module inserted in the cage (10G or 1G). A DRP controller is also implemented to dynamically configure the GTH transceiver and PLLs for 10G or 1G mode of operation.
4. **10G** Ethernet evaluation setup using the HTG-V6HXT-100G mated with HTG-SFP-PLUS-MDL extender module with one SPF module plugged into the first SFP+ cage.

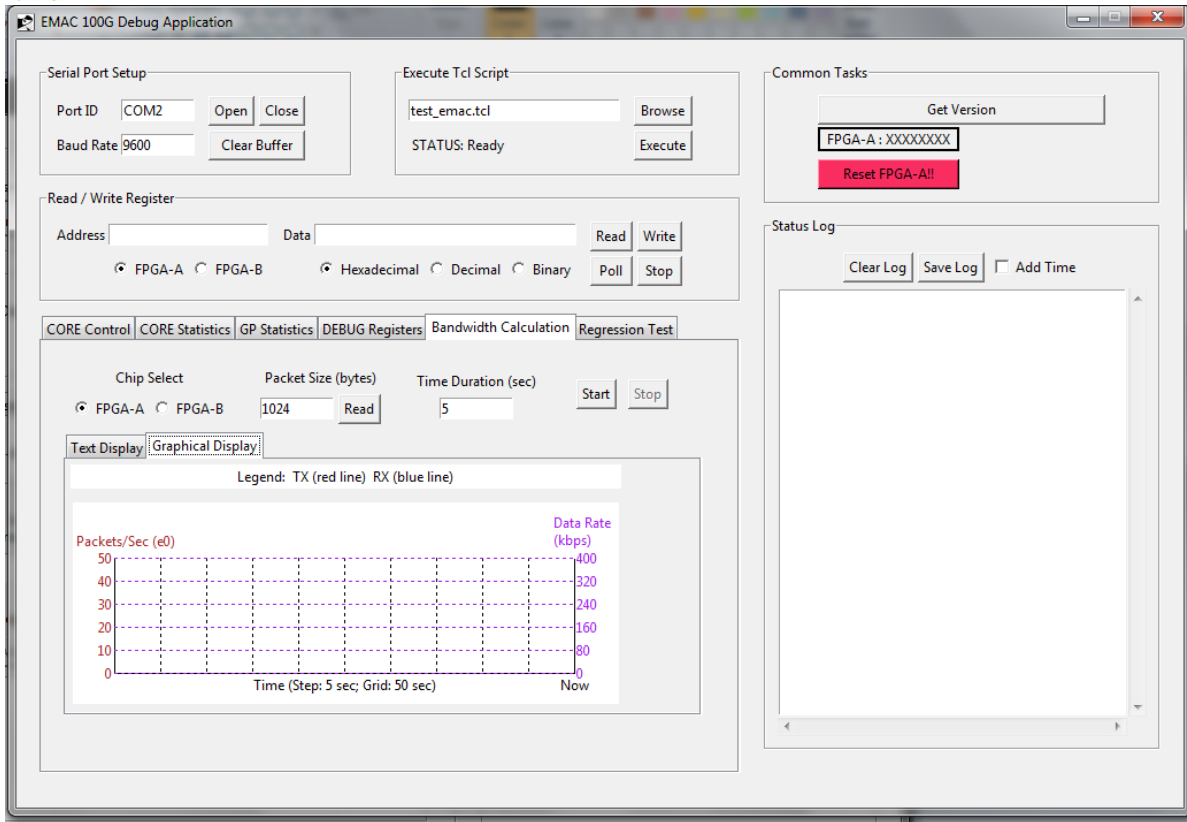
Each of the evaluation setup uses a line speed (up to 100Gbps) L2 Ethernet packet generator and checker along with the Ethernet (MAC/PCS) and interface cores required for each setup. The following is a generic block diagram for all evaluation and demonstration setups.

# Virtex 6 HXT 100G Ethernet Solutions

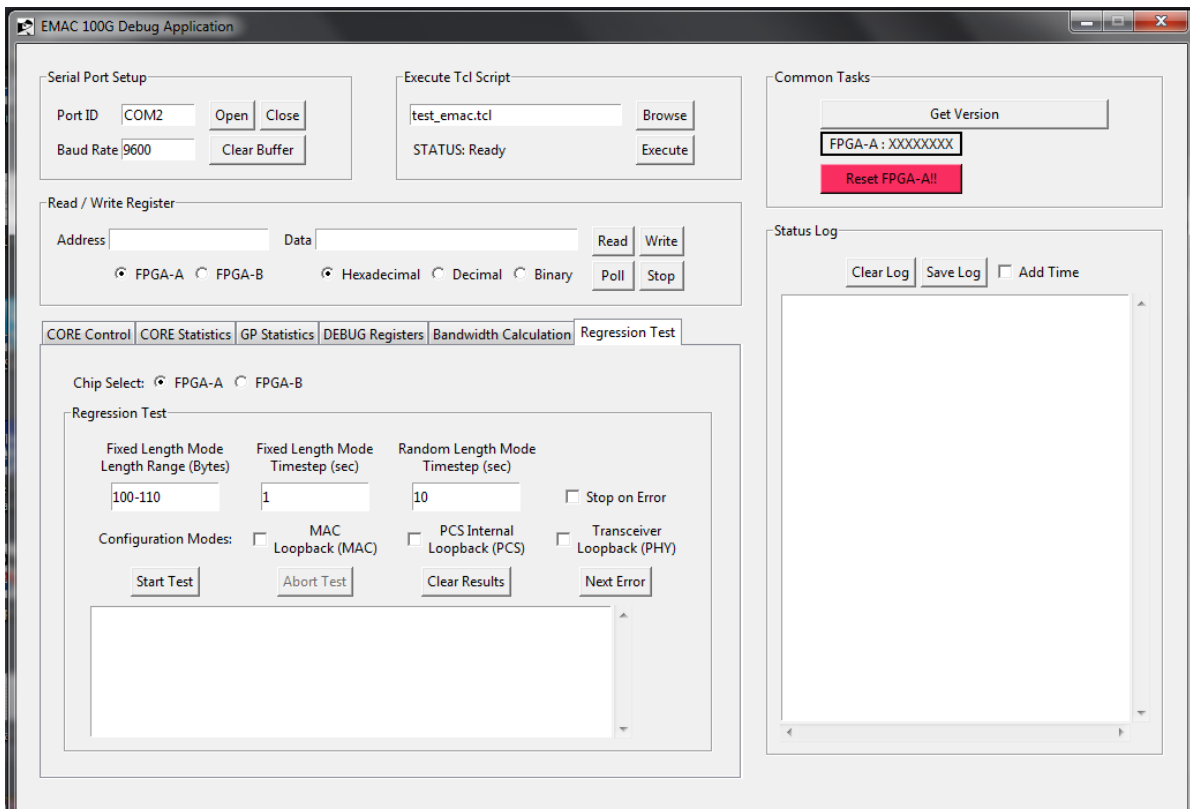


Following snap-shots shows the interface of the GUI application running on the PC.





The screenshot shows the 'EMAC 100G Debug Application' window. The 'Regression Test' tab is active. The 'Bandwidth Calculation' sub-tab is selected, displaying a line graph. The graph plots 'Packets/Sec (e0)' on the left y-axis (0 to 50) and 'Data Rate (kbps)' on the right y-axis (0 to 400) against 'Time (Step: 5 sec; Grid: 50 sec)' on the x-axis. A legend indicates TX (red line) and RX (blue line). The graph shows a steady increase in both metrics over time, with the data rate reaching approximately 320 kbps and packets per second reaching about 40.



The screenshot shows the 'EMAC 100G Debug Application' window with the 'Regression Test' sub-tab selected. The 'Regression Test' configuration panel is visible, showing the following settings:

- Chip Select:  FPGA-A  FPGA-B
- Fixed Length Mode Length Range (Bytes): 100-110
- Fixed Length Mode Timestep (sec): 1
- Random Length Mode Timestep (sec): 10
- Stop on Error:
- Configuration Modes:
  - MAC Loopback (MAC):
  - PCS Internal Loopback (PCS):
  - Transceiver Loopback (PHY):

Buttons for 'Start Test', 'Abort Test', 'Clear Results', and 'Next Error' are present at the bottom of the configuration panel.