



DS3/E3/STS-1 ATM TC CORE

PRODUCT BRIEF



1. INTRODUCTION

This document serves as product information for the ATM Transmission Convergence (TC) Core that implements up to 100 Mbps data-only ATM TC UNI functions. The document outlines the various features supported by the ATM TC core. It also includes the implementation summary for different devices of Altera.

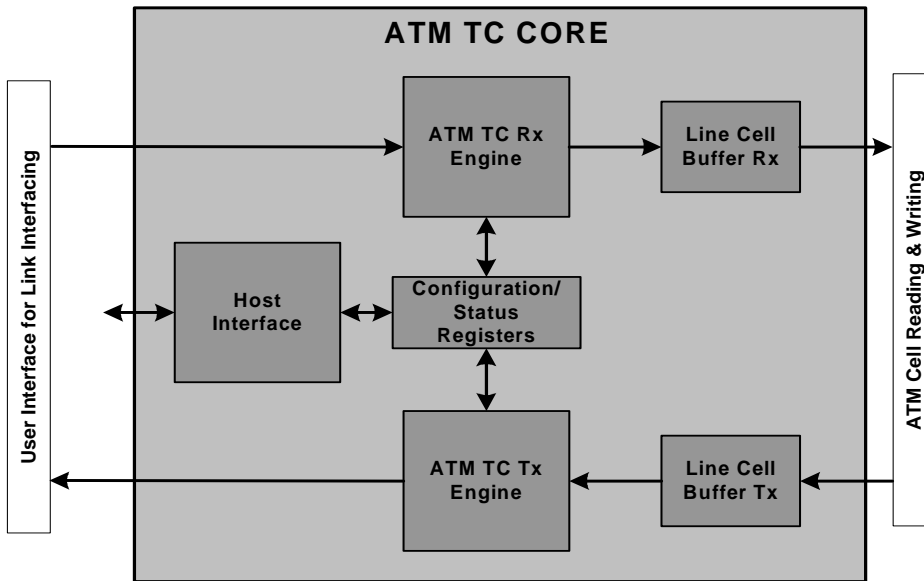
2. ATM TC CORE FEATURES

- The ATM-TC core can handle single DS3/E3/STS-1 line.
- Performs ATM Transmission Convergence (TC) Sublayer function on DS3/E3/STS-1 data.
- The core has serial data interface in case of DS3/E3, while it is 8-bit parallel data interface in case of STS-1.
- Performs cell delineation, HEC verification, payload de-scrambling and idle/unused cell filtering in RX direction, while HEC generation and payload scrambling is supported in TX direction.
- Generates Loss of Cell Delineation (LCD) 'start' and 'end' indications.
- Buffers ATM cells in both RX and TX directions.



3. ATM TC CORE BLOCK DIAGRAM

Illustration 1: ATM TC core block diagram





4. IMPLEMENTATION SUMMARY

An estimate of the logic resources and memory utilization for the DS3/E3/STS-1 ATM TC core for different devices of Altera is shown in the following table:

<i>Device</i>	<i>Speed Grade</i>	<i>Logic cells (LEs, ALUTs)</i>	<i>Registers</i>	<i>Memory M4K</i>
CYCLONE II	7	1222 LEs	775	2 M4Ks
STRATIX II	5	718 ALUTs	778	2 M4Ks

Table 1: DS3/E3/STS-1 ATM TC Core Implementation Summary

5. REFERENCES

1. PMC-Sierra, Inc.: PM8320 TEMUX 84E3 High Density T1/E1 Framer with Integrated VT/TU & DS3/E3 Mappers and M13 Multiplexer Data Sheet, Document No. PMC-2030446, Issue No. 4, December, 2003.
2. Exar Corporation: *T1/E1 Essentials White Paper* by Darren Pool, Document No. XRWP00001, 2007.
3. ITU-T, Recommendation I.432, B-ISDN User Network Interface – Physical Layer Specification, 03/93.