



40 Gigabit Ethernet MAC

(with ST-Avalon User Application Interface)

PRODUCT BRIEF



1. INTRODUCTION

This document serves as an introduction to the 40 Gigabit Ethernet MAC core. The document outlines the various features supported by the Ethernet MAC and a brief functional description of the core.

1.1. Glossary

LAN	Local Area Network
WAN	Wide Area Network
MAC	Media Access Controller
VLAN	Virtual LAN
EMAC	Ethernet MAC
RS	Reconciliation Sublayer
PHY	Physical Interface
CRC	Cyclic Redundancy Check
FCS	Frame Check Sequence
XLGMII	40 Gigabit Media Independent Interface
IFG	Inter-Frame Gap
DIC	Deficit Idle Count
MIB	Management Information Base
RMON	Remote Network Monitoring



2. 40G EMAC CORE FEATURES

The 40 Gigabit MAC core is designed to comply with the IEEE 802.3ba specifications, draft 1.1. The core is designed to support different configuration modes controlled by the core's register file. The core also provides support for IEEE managed objects, IETF MIB and RMON for management applications.

The 40G core at the user application interface, implements **Avalon Streaming Interface**, a simple and flexible interface, which is designed to transfer Ethernet frames to/from the MAC core. On the PHY side, the MAC core implements a 128-bit SDR (Single Data Rate) XLGMII interface for 40G MAC which samples frame data at rising edge of the clock. The 128-bit data from the MAC core can be directly connected to a compliant PCS core and then to 4-lane Transceivers with each lane operating @10.3125 Gbps.

The 40G core is designed for low logic utilization, implementing a narrow data path of 128-bit operating at 312.5 MHz.

The various core features are outlined below

- Implements the full 802.3 specification with preamble/SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively.
- Implements reconciliation sublayer functionality with start and terminate control characters alignment, error control character and fault sequence insertion and detection.
- Implements a 128-bit XLGMII interface operating at 312.5 MHz for 40G EMAC
- Implements Deficit Idle Count (DIC) mechanism to ensure maximum possible throughput at the transmit interface.
- Implements logic for padding of frames on the transmit path if the size of frame is less than 64 bytes.
- Implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention.
- Pause frame generation additionally controllable by user application offering flexible traffic flow control.
- Support for VLAN tagged frames according to IEEE 802.1Q.
- Support any type of Ethernet Frames such as SNAP / LLC, Ethernet II/DIX or IP traffic.
- Discards frames with mismatching destination address on receive (Except Broadcast and Multicast frames).
- Programmable Promiscuous mode to omit MAC destination address checking on receive EMAC.
- Optional multicast address filtering with 64-bit HASH Filtering table providing



imperfect filtering to reduce load on higher layers.

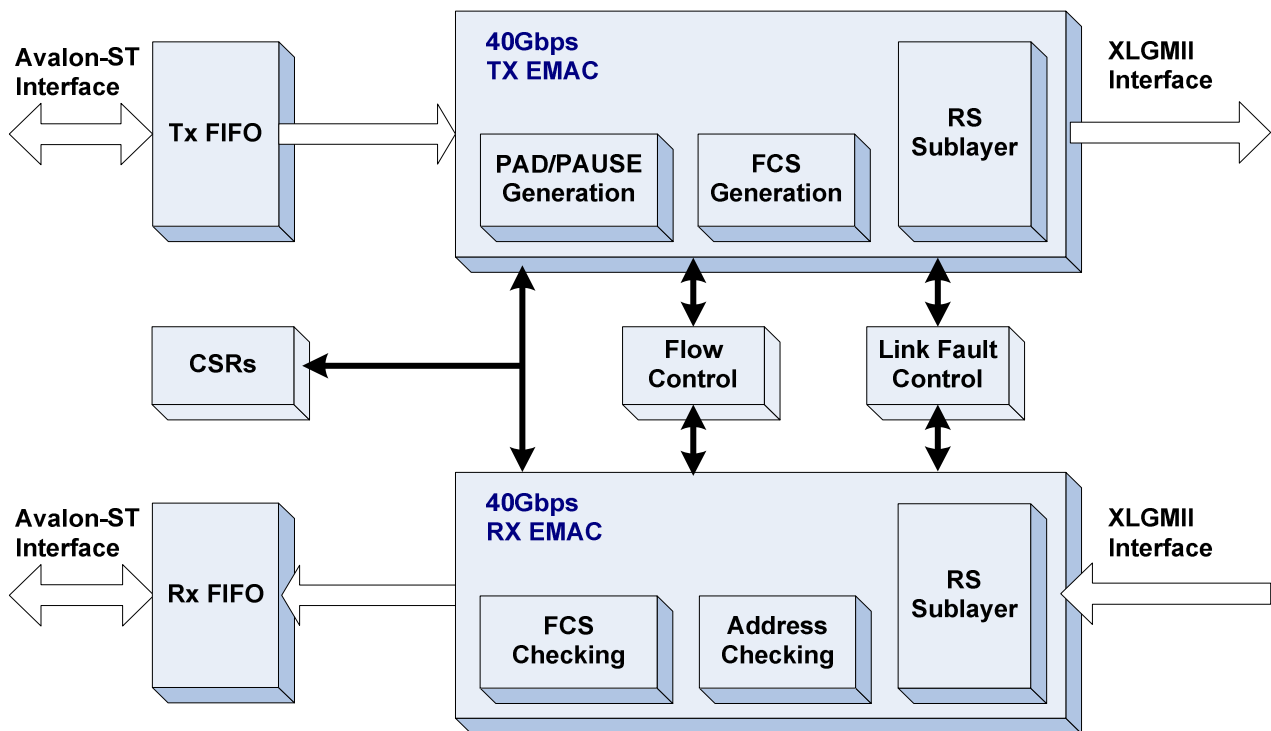
- CRC-32 generation and checking at high speed using an efficient pipelined CRC calculation algorithm.
- Implements logic for optional padding removal on RX path for NIC applications or forwarding of unmodified data to the user interface.
- Optional discard of runt frames (less than 64 Byte) at the core's reconciliation sublayer or forwarding of runt frames to the user application interface.
- Implements logic for optional forwarding of the CRC field to user application interface.
- Implements logic for optional forwarding of received pause frames to the user application interface.
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames).
- Status signals available with each Frame on the user interface providing information such as frame length, VLAN frame type indication and error information.
- Implements programmable internal XLGMII Loop-back.
- Implements statistics indicators for frame traffic as well as errors (alignment, CRC, length) and pause frames.
- Implements statistics and event signals providing support for 802.3 basic and mandatory managed objects as well as IETF Management Information Database (MIB) package (RFC 2665) and Remote Network Monitoring (RMON) required in SNMP environments.
- Implements Altera Avalon Streaming interface compliant user application interface. The application interface is designed as a 128-bit interface operating @ 312.5MHz.
- Implements Avalon Memory-Mapped host controller interface for accessing the core's register file.
- Implements MDIO Interface for accessing the PHY management and configuration registers.

3. FUNCTIONAL DESCRIPTION

3.1. Architectural Overview

The following figure shows the architecture for the 40 Gigabit Ethernet MAC

Figure 1: 10G EMAC High level block diagram





3.2. FUNCTIONAL OVERVIEW

3.2.1. Reconciliation Sublayer (RS) Operation

The RS layer is responsible to map the data to/from the MAC sublayer to the XLGMII interface. The RS layer provides a 128-bit interface at rising edge of XLGMII clock. The data is organized into 16 8-bit lanes with a control bit available for each lane.

3.2.2. MAC Sublayer Operation

The MAC sublayer is responsible to perform transmit and receive media access control (MAC) operations. The transmit MAC block transmits frames from a user application interface to the reconciliation sublayer, which then transmits these frames to the XLGMII physical interface. The receive MAC block receives Ethernet frames from the reconciliation sublayer, validates the Ethernet frame and transfers this frame to the user application interface. The following description defines the various functions performed by transmit and receive Ethernet MAC engines.

3.2.2.1. Transmit Ethernet MAC

The transmit Ethernet MAC performs the following main functions

- Accepts data including Destination Address, Source Address and length field from the MAC client.
- Appends preamble and SFD to the Ethernet frames.
- Pads the incoming frames from the user application interface to minimum frame size (64 Byte) whenever the frame size is less than 64 Byte.
- Calculates and Appends proper FCS (CRC-32) value to outgoing frames and verifies full octet boundary alignment.
- Delays transmission of frame data for specified inter-frame gap period.
- Controls Inter-frame gap timing by maintaining a Deficit Idle Count value between 0 - 7
- Inserts start and terminate control characters before frame transmission.
- Inserts Idle control characters between frames (Inter-frame gap) or when there are no frames available for transmission.
- Manages local device flow control by generating PAUSE control frames.
- Manages Remote device congestion by transiting to HALT state for a specified time quanta.



3.2.2.2. Receive Ethernet MAC

The receive Ethernet MAC performs the following main functions

- Receives a frame from the RS sub layer via a 128-bit data bus.
- Presents to the MAC client sublayer frames that are either frames with group address or directly addressed to the local station (Address recognition).
- Filters Multi-cast frames using hash filtering algorithm.
- Discards all frames not addressed to the receiving station when promiscuous mode is disabled.
- Accepts all frames destined to the EMAC if promiscuous mode is enabled.
- Checks incoming frames for transmission errors by way of FCS and verifies octet boundary alignment.
- Discards received transmissions that are less than a minimum length (64 bytes) at the core's reconciliation sublayer
- Truncates frames with length greater than maximum frame length when Jumbo frames are not allowed to pass through.
- Optionally forwards pause frames to user application.

3.2.3. MAC Flow Control Operation

The MAC flow control block is responsible to maintain a proper flow of Ethernet frames through transmit and receive engines. It performs the following main functions

- Prevents the receive EMAC FIFO congestion by sending pause control frames.
- Prevents the remote device congestion by responding to pause frames and going into idle state for specified number of slot times.



4. MANAGEMENT INTERFACE

The 40G EMAC core provides a set of signals which can be used to implement the statistics required in IEEE 802.3 basic, mandatory and recommended Management information packages. In addition the MAC core provides signals to generate the applicable objects of the Management Information Database (MIB, MIB II) according to IETF RFC2665.

5. 40G EMAC IMPLEMENTATION

The core has been targeted to Altera StratixIV (-C3 for 40G EMAC) device. An estimate for the core utilization is given in the following table

Table 5-1 40G EMAC Resource Utilization Estimate

ALUTS	4,500
Registers	6,000
RAM (M9K Blocks)	22

6. REFERENCES

1. IEEE 802.3ba specifications, Draft 1.1
2. RFC2665, definition of Managed Objects for Ethernet Like Interface Type, www.ietf.org
3. RFC2863, The Interface Group MIB, www.ietf.org
4. RFC2819, Remote Network Monitoring (RMON) MIB, www.ietf.org