



**STRUCTURED/UNSTRUCTURED AAL1 IWF CORE**

**PRODUCT BRIEF**



## 1. INTRODUCTION

This document serves as product info for the multi-channel time-sliced AAL1 IWF core. The core is configurable for 8/16/32 lines and support both structured and unstructured modes of operations. In structured mode, two groups are supported based on T1/E1 slot mapping. In unstructured mode, all T1/E1 slots constitute one group.

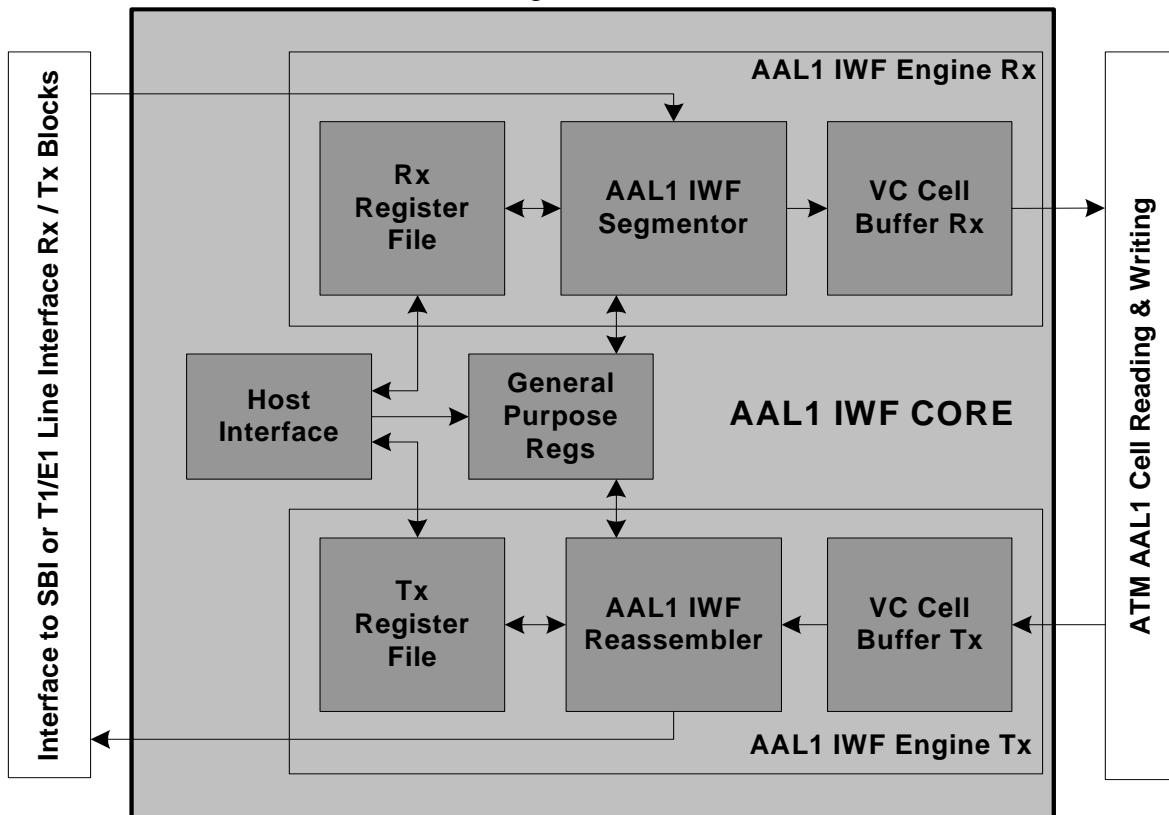
## 2. AAL1 IWF CORE FEATURES

- Supports packing (segmentation) and unpacking (reassembly) of ATM cells for 8/16/32 T1/E1 full duplex lines.
- Updates sequence number per virtual channel (VC).
- Maintains pointer field per VC for structured data transfer (SDT).
- Supports 2/4 groups per line for structured data transfer.
- Extracts T1/E1 user data from AAL1 cells including the sequence number and checking is based upon 'Robust' or 'Fast' algorithms.
- Deep buffering of T1/E1 transmit data bytes to accommodate 16 ms of cell delay variation (CDV).
- Buffers ATM cells in both RX and TX directions.
- Generates partially filled cells for reducing assembly delay at the expense of greater cell rate in RX direction.
- TDM side of the core can either be connected to SBI interface or the T1/E1 Line Interface. On ATM side the core is interfaced to a UTOPIA bus.



### 3. AAL1 IWF CORE BLOCK DIAGRAM

Illustration 1: AAL1 IWF Core block diagram





## 4. IMPLEMENTATION SUMMARY

An estimate of the logic resources and memory utilization for the 8/16/32 lines unstructured AAL1 IWF core for different devices of Altera is shown in the following table:

<i>Device</i>	<i>Core Type</i>	<i>Speed Grade</i>	<i>Logic cells (LE)</i>	<i>Registers</i>	<i>Memory M4K</i>	<i>Performance MHz</i>
CYCLONE III	32 Lines	7	5983 LEs	2155	41 M4K	144 MHz
CYCLONE III	16 Lines	7	4118 LEs	1855	28 M4K	148 MHz
CYCLONE III	8 Lines	7	3117 LEs	1693	22 M4K	150 MHz

*Table 1: AAL1 IWF Implementation summary*

## 5. REFERENCES

1. ATM Forum: Circuit Emulation Service Interoperability Specification, af-vtoa-0078\_000, Jan 1997.
2. Exar Corporation: *T1/E1 Essentials White Paper* by Darren Pool, Document No. XRWP00001, 2007.
3. PMC-Sierra, Inc.: PM73122 AAL1gator-32 ATM Adaptation Layer 1 Segmentation and Reassembly Processor-32 Data Sheet, Document No. PMC-1981419, Issue 8, May 2002.
4. ITU-T, Recommendation I.361, B-ISDN ATM Layer Specification, 02/99. ITU-T, Recommendation I.361-1, B-ISDN ATM Layer Specification: Type 1 AAL, 08/96.
5. ITU-T, Recommendation I.432, B-ISDN User Network Interface – Physical Layer Specification, 03/93.