



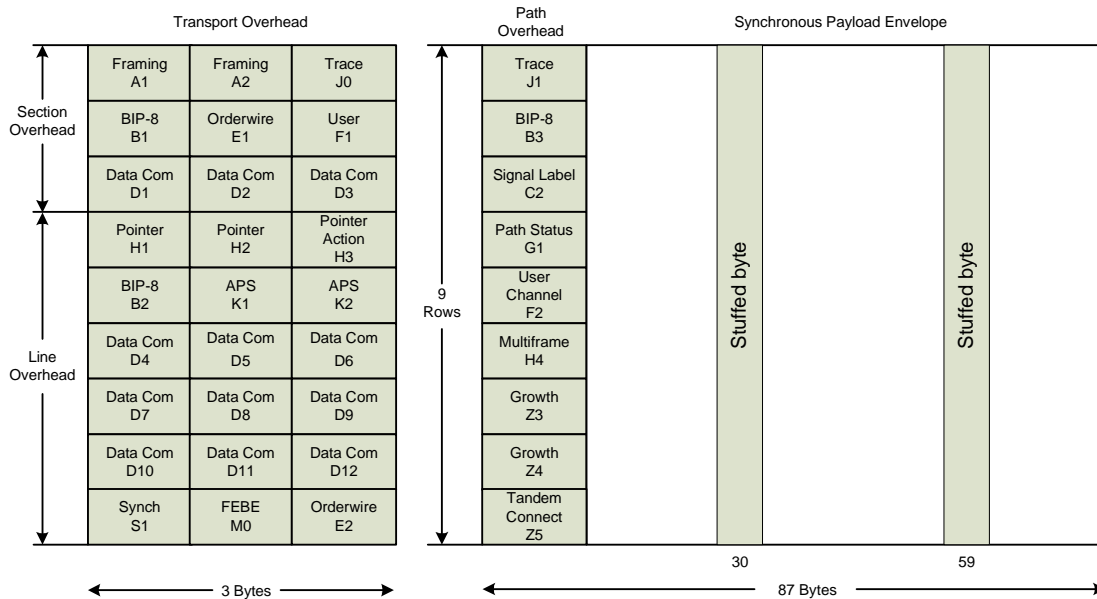
# **STS-1/STM-0 Framer**

**PRODUCT BRIEF**





**Figure 2: STS-1/STM-0 Mode Frame Structure**



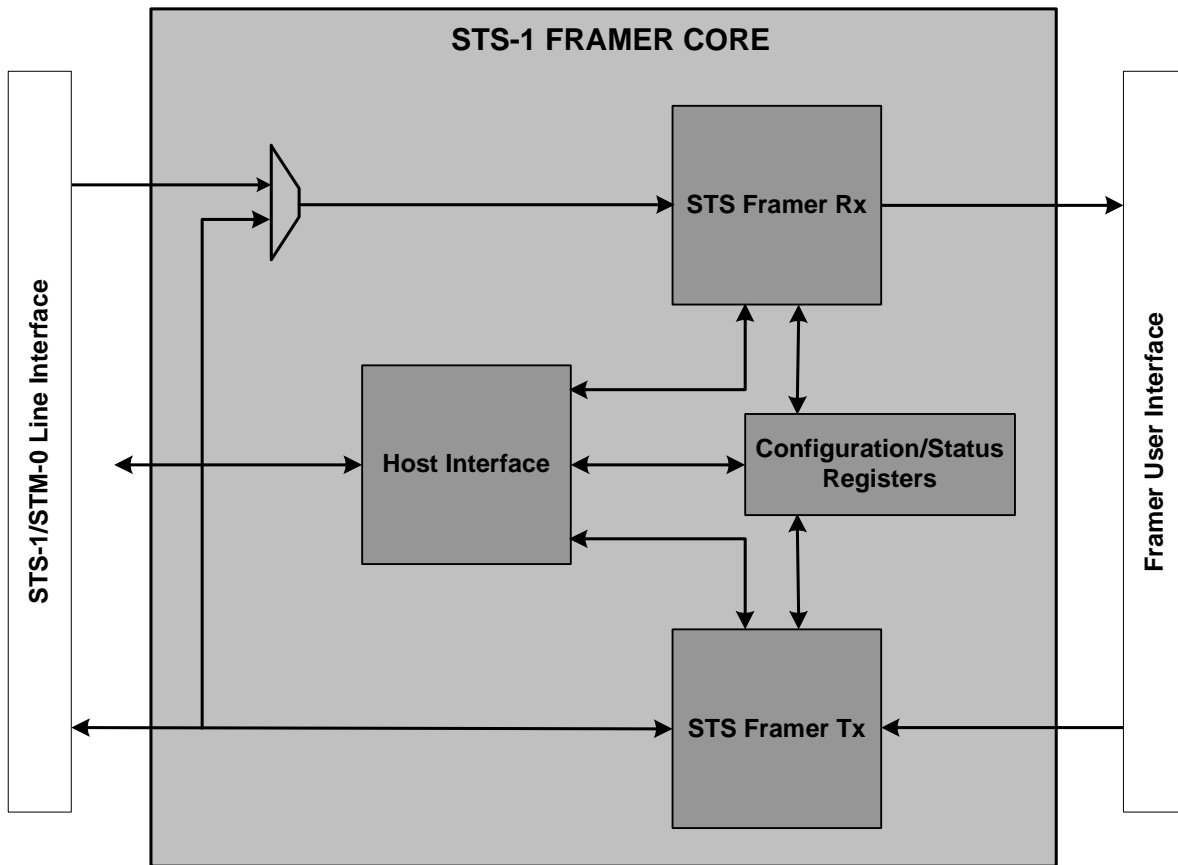
## 2. STS-1/STM-0 FRAMER CORE FEATURES

- The STS-1/STM-0 framer is designed to process single STS-1/STM-0 stream.
- Implementation of complete pointer processing, payload extraction and stuff bytes removal in RX direction.
- Detection of BIP errors in RX direction and optional error reporting in reverse direction.
- Detection of TOH and POH alarms/defects/errors and interrupt-generation with optional error reporting in reverse direction.
- Processing of both section and path trace messages in RX direction.
- Configurable overhead generation, scrambling and Bit Interleaved Parity(BIP) calculations in TX direction.
- Locked payload generation in TX direction with optional stuff column insertion.
- In RX direction, the framer receives SONET/SDH frames serially from the external interface.
- In TX direction, the framer receives parallel payload data bytes.



### 3. STS-1/STM-0 FRAMER CORE BLOCK DIAGRAM

Figure 3: STS-1/STM-0 Framer Core Block Diagram





## 4. DEVICE USAGE SUMMARY

An estimate of the logic resources and memory utilization for the STS-1/STM-0 Framer for different devices of Altera and Xilinx are shown in Table 1 and 2 respectively.

<i>Device</i>	<i>Speed Grade</i>	<i>Logic cells (LE)</i>	<i>Registers</i>	<i>Memory M4K, M9K</i>	<i>Performance MHz</i>
CYCLONE II	-7	2700 LEs	1698	4 M4K	100 MHz
CYCLONE III	-7	2700 LEs	1698	4 M9K	110 MHz

*Table 1: Framer device usage summary for Altera FPGA's*

<i>Device</i>	<i>Speed Grade</i>	<i>Logic cells (LUTs)</i>	<i>Registers</i>	<i>Slices</i>	<i>Memory 18k BlockRAM</i>	<i>Performance MHz</i>
SPARTAN 3E	-4	1793 LUTs	1752	1642	4	210 MHz
VIRTEX 4	-10	1805 LUTs	1752	1636	4	184 MHz
VIRTEX 5	-1	1544 LUTs	1791	911	4	238 MHz

*Table 2: Framer device usage summary for Xilinx FPGA's*

## 5. REFERENCES

1. PMC-Sierra, ARROW 155 ASSP Telecom Standard Product Data Sheet
2. Mindspeed, CX28250 ATM Physical Interface Devices Data Sheet