UTOPIA LEVEL-2 MASTER

PRODUCT BRIEF

1. INTRODUCTION

This document serves as an introduction to the Utopia Level 2 Master core. The document outlines the various features supported by the Utopia Level 2 Master core. It also includes the implementation summary of the Utopia Level 2 Master on different devices.

2. UTOPIA MASTER CORE FEATURES

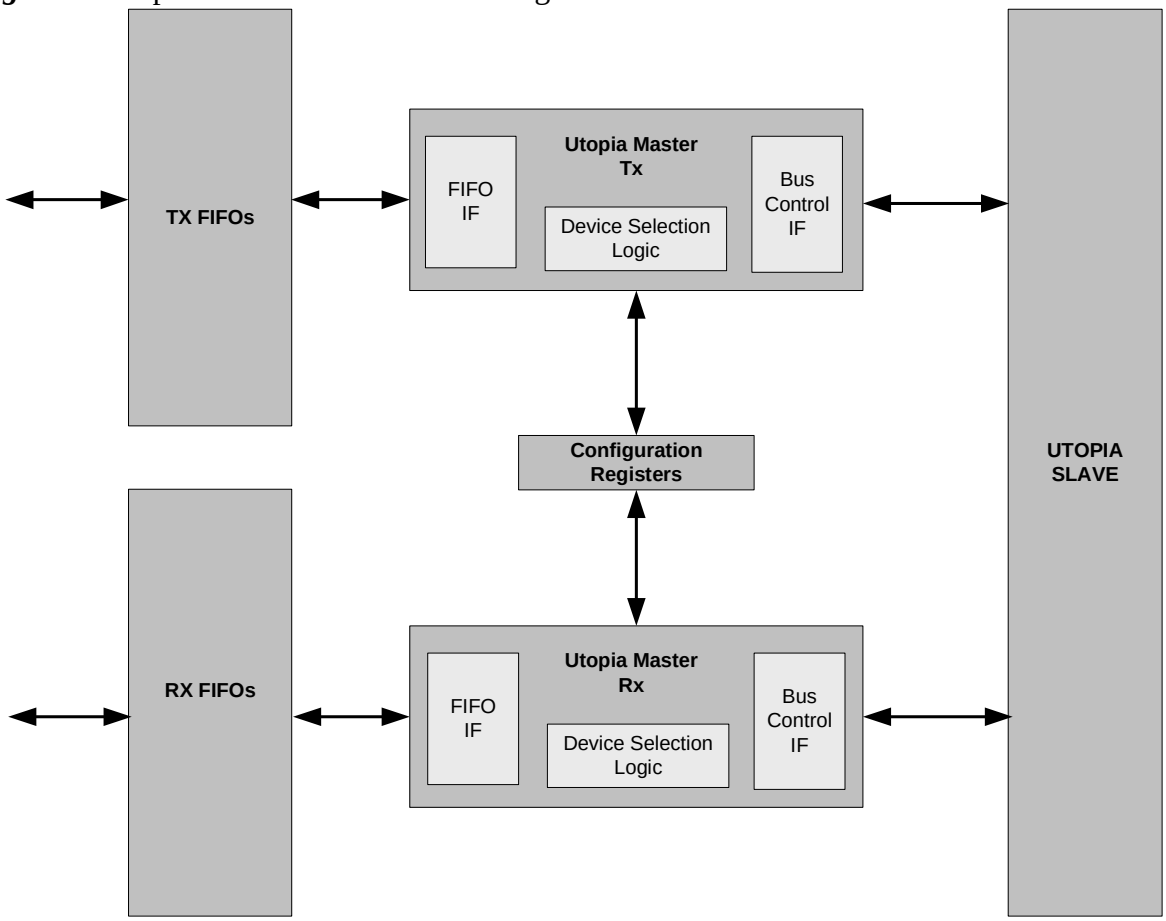
The Utopia Master core is designed to comply with Utopia Level 2, Version 1.0 specifications. The core is designed to support both 8 and 16 bit mode operation. The simple FIFO interface is provided for both receive and transmit blocks.

The various features of the core are outlined below:

- Conforms to UTOPIA level 2, Version 1.0 Specification.
- 8/16 bit UTOPIA bus operation.
- Supports up to maximum of 31 PHYs.
- Single Physical Layer Operation, with cell-level handshaking.
- Multi-PHY(MPHY) operation ,with a single *clav* signal.
- Configurable PHYs through a register.
- Round robin PHY Selection Scheme.
- Internal Cell Based FIFOs for both Receive and Transmit Blocks.
- FIFO reading and writing interface for Rx and Tx respectively.
- Includes Simulation Models for the ModelSim Simulation Tools.

3. UTOPIA LEVEL-2 MASTER BLOCK DIAGRAM

Figure 1: Utopia Level-2 Master Block Diagram



4. DEVICE USAGE SUMMARY

An estimate of the logic resources and memory utilization for the Utopia Level 2 Master for Altera device is shown in the following table. The Utopia Master core contains two main blocks Rx and Tx and Cell based FIFOs for both Transmit and Receive blocks. The following tables give the implementation of the Rx and Tx Blocks with the maximum FIFOs for the Utopia Level 2 Master. The first table gives the resource usage for the Utopia Rx and Tx Blocks and the second tables give the resource usage for FIFOs. These tables give the maximum resource that could be utilized by a Utopia Level 2 Master for 31 PHYs.

Device	***Speed Grade***	***Logic cells (LE)***	***Performance MHz***
CYCLONE II	-8	1387 LEs	81 MHz

Table 1: Utopia Master logic resource usage summary for Altera FPGA's

Device	***Speed Grade***	***Logic cells (LE)***	***Performance MHz***
CYCLONE II	-8	3873LEs	32

Table 2: Utopia Master FIFO resource usage summary for Altera FPGA's

5. REFERENCES

1. ATM Technical Committee: Utopia Level 2, Version 1.0, af-phy-0039.000, June 1995.