



UTOPIA LEVEL-2 SLAVE

PRODUCT BRIEF



1. INTRODUCTION

This document serves as an introduction to the Utopia Level 2 Slave core. The document outlines the various features supported by the Utopia Level 2 Slave core. It also includes the implementation summary of the Utopia Level 2 Slave on different devices.

2. UTOPIA SLAVE CORE FEATURES

The utopia slave core is designed to comply with Utopia Level 2, Version 1.0 specifications. The core is designed to support both 8 and 16 bit mode operation. The simple FIFO interface is provided for both receive and transmit blocks.

The various features of the core are outlined below:

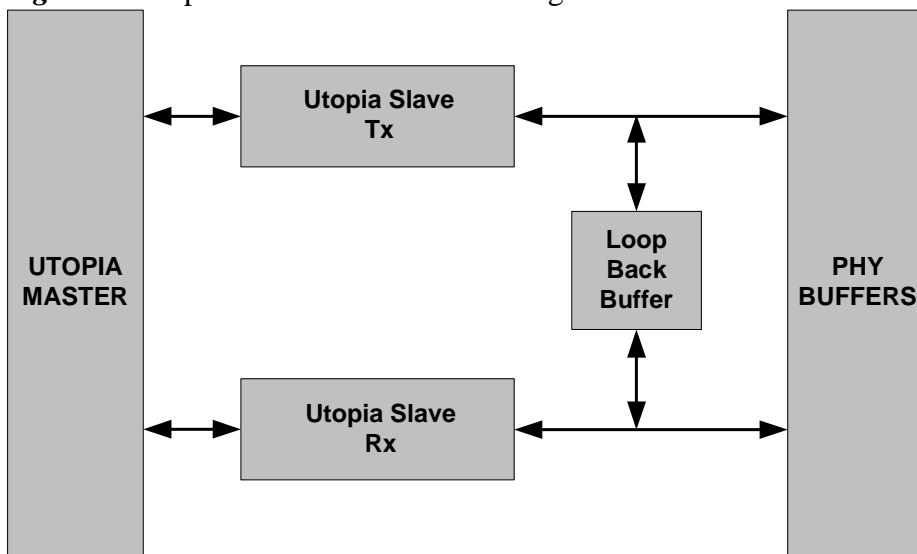
- Conforms to UTOPIA level 2, Version 1.0 Specification.
- 8/16 bit UTOPIA bus operation.
- Supports upto maximum of 31 PHYs.
- Single Physical Layer Operation, with cell-level handshaking.
- Multi-PHY(MPHY) operation, with a single *clav* signal.
- Loop-back mode support from transmit to receive.
- FIFO reading and writing interface for Rx and Tx respectively.
- Includes Simulation Models for the ModelSim Simulation Tools.



3. UTOPIA LEVEL-2 SLAVE BLOCK DIAGRAM

The following figure shows the high level block diagram for Utopia Level-2 Slave core.

Figure 1: Utopia Level-2 Slave Block Diagram





4. DEVICE USAGE SUMMARY

An estimate of the logic resources and memory utilization for the Utopia Level 2 Slave for different devices of Altera is shown in the following table. The Utopia Slave core contains two main blocks Rx and Tx and a loop-back buffer. The resource usage for the buffer depends upon the number of PHY available. The following table gives the implementation of the Rx and Tx Blocks for the Utopia Level 2 Slave.

<i>Device</i>	<i>Speed Grade</i>	<i>Logic cells (LE)</i>	<i>Registers</i>	<i>Performance MHz</i>
STRATIX	-8	166 LEs	38	144 MHz
CYCLONE II	-8	144 LEs	38	155 Mhz

Table 1: Utopia slave (transmit side) device usage summary for Altera FPGA's

<i>Device</i>	<i>Speed Grade</i>	<i>Logic cells (LE)</i>	<i>Registers</i>	<i>Performance MHz</i>
STRATIX	-8	231 LEs	23	103 MHz
CYCLONE II	-8	232 LEs	23	105 Mhz

Table 2: Utopia slave (receive side) device usage summary for Altera FPGA's

5. REFERENCES

1. ATM Technical Committee: Utopia Level 2, Version 1.0, af-phy-0039.000, June 1995.