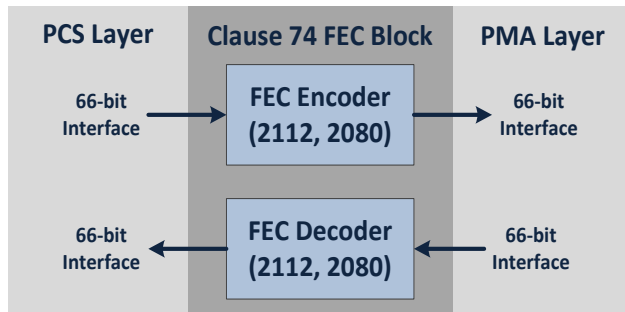


IEEE 802.3 Clause 74 FEC IP Core

Product Brief (HTK-CLAUSE74-FEC)



The Forward Error Correction (FEC) IP core is designed to comply with the Clause 74 (FEC sublayer for 10GBASE-R, 40GBASE-R, and 100GBASE-R PHYs) of the IEEE 802.3-2008/IEEE 802.3ba-2010 specifications. As shown in the figure, cyclic code (2112, 2080) FEC block lies between PCS and PMA sublayers and provides coding gain to increase the link budget and BER performance.



FEC is the optional error correction specified for:

- 10GBASE-KR PMD for 10Gbps backplane
- 40GBASE-KR4 PMD for 40Gbps backplane
- 40GBASE-CR4 and 100GBASE-CR10 PMDs for 40Gbps and 100Gbps copper cable attachment

For a PHY with a multi-lane BASE-R PCS, the FEC sublayer is instantiated for each PCS lane and operates autonomously on a per PCS lane basis. Thus, FEC sublayer operates at 10.3125Gbps on each BASE-R PCS lane at the service interface for 10G and 40G; and 5.15625Gbps for 100G.

The FEC IP core is provided as two blocks, an encoder and a decoder, as an implementation of the error correction algorithm for a 66-bit interface, i.e. 66-bit in and 66-bit word out.

The encoder takes in the 66 bit word (2 Sync bits +64-bit data) and outputs an encoded 66-bit word. The encoder works over a frame of 32 66-bit words and outputs the encoded data along with parity as 32 by 66-bit words. The encoder does three tasks to the data: sync bits compression in each 66-bit word, parity generation and final scrambling of the data stream.

For the decoder, there are five tasks: a bit slip function, the three encoder tasks in reverse and the final error correction. The bit slip block ensures that the misaligned data stream on receiver side are aligned properly using a single bit slip at a time per frame. The decoder recovers the data frame and signals it as uncorrectable or corrected. The uncorrected signal to the bit slip block results in one more bit slip in the output data frame. Once the corrected signal is received, the bit slip block stops shifting and locks at the last bit slip. Four such subsequent frames that are decoded as correct, result in the sync flag going high, thus indicating bit lock has been completed.

Features Overview

- Implements an FEC IP core compliant with the clause 74 of the IEEE 802.3-2008 and IEEE 802.3ba-2010 specifications.
- Implements a 66-bit streaming interface
- Implements a 66b/65b sync bits compression and decompression in FEC transmit and receive paths respectively.
- Implements a (2112, 2080) shortened fire (cyclic) code encoder and decoder based on 802.3ba specified polynomial $x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$. The 2112 bits are in the format of 32 66-bit words.
- Implements the pseudo noise generator for scrambling the generated codeword based on the polynomial $x^{58} + x^{39} + 1$. The reverse is done in the FEC RX path.
- The decoder also has an extra bit slip block to make sure the FEC decoder gets the aligned frame. Until the alignment is reached, the bit slip block continues to receive “uncorrectable signal” from the decoder. Once correct frame is determined for 4 consecutive frames, the bit slip locks the bit slip position and the decoder asserts the sync bit high.
- Streaming design allows easy integration in PCS layers.
- Only the decoder requires memory for error correction.
- Implements cyclic error correcting code (2112, 2080) compliant with IEEE 802.3ba Specifications.
- Decoder can correct single burst error of up to 11 bits with 53 40-bit words or 32 66-bit words or 2112 bits.
- Implements block synchronization and pseudo-random noise scrambling as described in 802.3ba specifications.
- Encoder and pseudo random noise generator is test with test cases provided in 802.3ba specification.
- Error correction capability and block synchronization is tested on hardware with 40G PCS and MAC with more than 1,000 random scenarios.
- Supports streaming interface.

See **Appendix A** for functional details of FEC.

IEEE 802.3 Clause 74 FEC IP Core

Product Brief (HTK-CLAUSE74-FEC)



Resource Utilization

The core utilization summary for the FEC IP is given in following tables.

IEEE 802.3 Clause 74 FEC - Resource Usage for Xilinx Devices

<i>Device</i>	<i>Module</i>	<i>Slices</i>	<i>Slice LUTS</i>	<i>Slice Registers</i>	<i>Memory 18k/36k BRAM</i>
Virtex-6 (-2C Speed)	Encoder	253	681	371	0
	Decoder	709	2061	1723	1 – 36k BRAM

IEEE 802.3 Clause 74 FEC - Resource Usage for Altera Devices

<i>Device</i>	<i>Module</i>	<i>COMB. ALUTs</i>	<i>Memory ALUTs</i>	<i>Registers</i>	<i>Memory M9K</i>
Stratix-IV (-2C Speed)	Encoder	701	0	368	0
	Decoder	1976	0	1622	2

Deliverables

- Compiled synthesizable binaries or synthesizable source code (Verilog); depending upon license type
- Test bench in system Verilog with random frame data and error injection
- Behavioral Model
- Golden test vectors from standard
- User Documentation
- Synthesis scripts for multi platform FPGA

Optional Features

The FEC core can also be supplied with necessary modifications with the following features:

- Customizable data path (e.g. 33-bit data path)
- Error logging to analyze error pattern over time
- Additional random error correction block to allow errors more than 11 bits apart.

In addition, any cyclic code encoder/decoder customized implementation can also be provided.

Licensing and Maintenance

- ***NO yearly maintenance fees for upgrades and bug fixes***
- Basic core licensing for a single vendor (either Xilinx or Altera) compiled (synthesized netlist) binary
- Vendor and device family agnostic source code (Verilog) license option also available

Contact and Sales Information

For sales, contact Mantaro Networks, Inc at:

Phone: +1-301-528-2244

Email: sales@mantaro.com

A. Functional Overview

A.1 FEC Encoder

The block diagram of FEC encoder is given in Figure 1. The FEC encoder takes 32 x 66-bit blocks and encodes it into a single FEC block of 2112 bits. The FEC encoder compresses the two sync bits to one transcode bit which is further xored with the bit 8 of the corresponding 66-bit clock. The resulting 2080 bits are fed to the (2112, 2080) encoder. The encoder divides the incoming 66-bits block from LSB side and produces 32-bit parity. The parity bits are stitched at the last 66-bits encoded block. This code, (2112, 2080) is a shortened cyclic code. The generator polynomial for this code is given in equation below.

$$G(x) = x^{32} + x^{23} + x^{21} + x^{11} + x^2 + 1$$

The FEC block is scrambled with PN-2112 Pseudo-noise generator and then sent to the PMA interface. The latency of encoder from first 66-bit input block to the first 66-bit output block is 4 cycles.

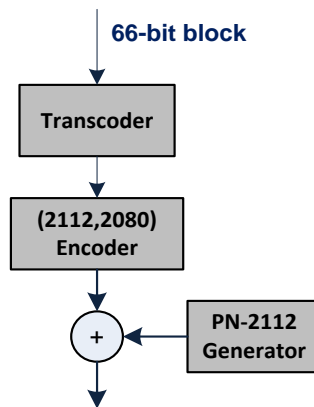


Figure 1. FEC Encoder Blocks

The FEC encoder module's interface I/Os are shown in Figure 2.

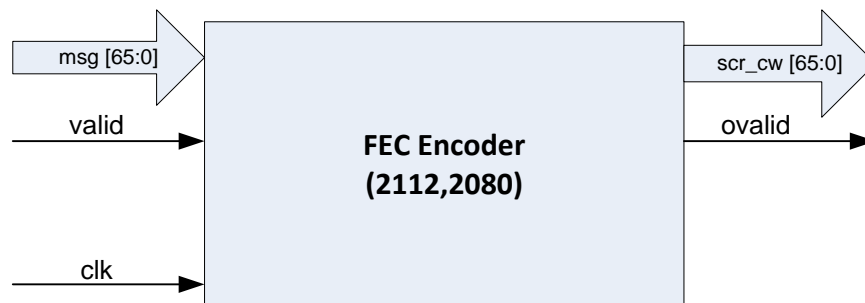


Figure 2. Encoder Interface I/O

A.2 FEC Decoder

Block diagram of the FEC decoder is given in Figure 3. FEC decoder corrects burst errors up to 11-bits. FEC decoder also establishes block synchronization based upon repeated decoding of received sequences as described in IEEE 802.3ba specification. FEC decoder receives 66x32-bits blocks, descrambles it using PN-2112 generator, decodes and corrects for possible errors in the frame.

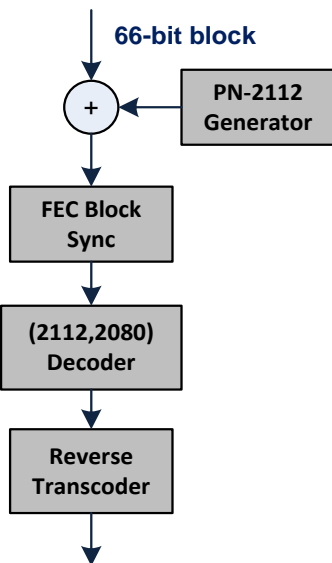


Figure 3. FEC Decoder Blocks

The FEC decoder module's interface I/Os are shown in Figure 4.

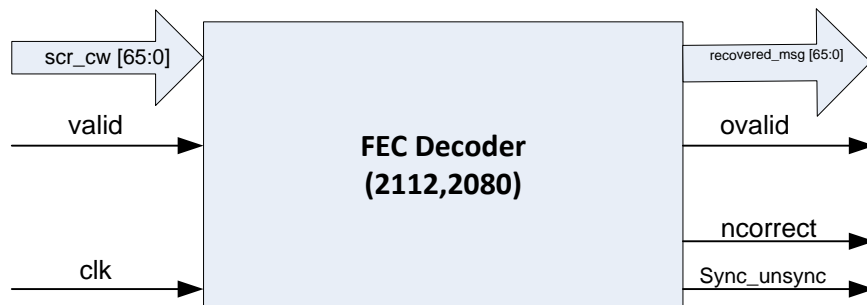


Figure 4. Decoder Interface I/O

A.2.1 FEC Block Synchronization

The FEC block synchronization is achieved by using conventional n/m locking technique as described below.

- I. Test for a potential candidate block start position.
 - a. Descramble block using PN-2112 generator.
 - b. If the codeword can't be corrected, shift one bit position and then retry.
- II. If the codeword is correctable then search for 4 consecutive blocks.
 - a. If any of them fails, shift one bit position and restart counting.
 - b. If 4 consecutive blocks are received with good parity, declare block sync.
- III. Block sync is established.
- IV. If 8 consecutive uncorrectable blocks are received, drop sync and restart from point I.