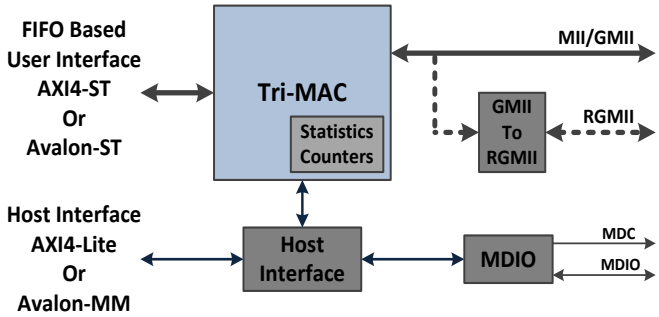
10/100/GiGE Triple-Speed MAC

Product Brief (HTK-TRI-MAC-8)

The 10/100/1000Mbps Tri-mode Ethernet MAC offers an IEEE802.3-2015 compliant solution that meets the requirements for tri-mode LAN in NIC (Network Interface Card) applications.

As shown in figure, the 10/100/1000Mbps MAC IP includes:

- AXI4-Streaming or Avalon-Streaming, FIFO based user side interface
- Triple speed MAC with MII/GMII PCS side interface and a simple FIFO based user side interface
- GMII to RGMII interface wrapper
- Statistics counter block (for RMON and MIB)
- MDIO cores for external PHY status/control



A complete reference design using a simple L2 (MAC level) packet generator/checker is also included to facilitate quick integration of the Ethernet MAC in a user design. An example design and top level wrapper is provided to connect the Tri-MAC core to the popular Marvell 88E1111 Ethernet PHY.

MAC core is designed with 8-bit data path operating at 2.5, 25, and 125MHz for 10Mbps, 100Mbps and GiGE Ethernet modes respectively.

Ethernet IP solution implements two user (application) side interfaces. The register access port is a 32-bit AXI4-Lite or Avalon-MM interface. The Ethernet user application interface is provided through 32-bit FIFOs with a simple handshake mechanism. FIFO clock interface is fixed at 125MHz clock rate for all modes of operation.

On the Physical interface side, the MAC core implements an 8-bit SDR (Single Data Rate) GMII for GiGE mode of operation and 4-bit SDR MII interface for 10/100Mbps mode of operation.

Features Overview

- Implements the full 802.3 specification with preamble / SFD generation, frame padding generation, CRC generation and checking on transmit and receive respectively.
- Dynamically configurable to support 10Mbps, 100Mbps or 1000Mbps operation
- Support for 10/100Mbps full duplex or half duplex operation and 1000Mbps full duplex mode selectable via a Core configuration option
- Seamless interface to commercial Ethernet PHY device via an 8-Bit GMII or 4-Bit RGMII interface operating at 125MHz for GiGE mode and via a 4-Bit MII interface operating at 25/2.5MHz for 100/10Mbps modes
- When operating in Full Duplex mode, implements fully automated XON and XOFF Pause Frame (802.3 Annex 31A) generation and termination providing flow control without user application intervention
- Pause frame generation additionally controllable by user application for traffic flow control
- In half-duplex mode, provides full collision support, including jamming, back-off, and automatic retransmission
- Support for VLAN tagged frames according to IEEE 802.1Q.
- Support any type of Ethernet Frames such as SNAP/LLC, Ethernet-II/DIX and VLAN tagged frames.
- Programmable MAC address filtering; discards frames with mismatching destination address on receive (Except Broadcast and frames)
- Programmable Promiscuous mode support to omit MAC destination address checking on receive Multicast address filtering on receive based on 64 entries hash table reducing higher layer processing load
- Optional multi-cast address filtering with 64-bit HASH Filtering table providing imperfect filtering to reduce load on higher layers
- Programmable frame maximum length providing support for any standard or proprietary frame length (e.g. 9K-Bytes Jumbo Frames)
- Status word available with each Frame on the user interface providing information such as frame length, VLAN frame type indication and error information
- Optional padding termination on RX path for NIC applications or forwarding of unmodified data to the user interface
- Internal GMII/MII Loop-back

- Statistics indicators for frame traffic as well as errors (alignment, CRC, length) and pause frames
- Simple handshake user application FIFO interface with programmable threshold levels ensuring data rates of 1Gbps with full back-to-back frame transfer support
- Implements statistics and event signals providing support for 802.3 basic and mandatory managed objects as well as IETF Management Information Database (MIB) package (RFC 2665) and Remote Network Monitoring (RMON) required in SNMP environments.

Licensing and Maintenance

- ***NO yearly maintenance fees for upgrades and bug fixes***
- Basic core licensing for a single vendor (either Xilinx or Altera) compiled (synthesized netlist) binary

Deliverables

- Compiled synthesizable binaries for the MAC core
- Source code RTL (Verilog) MDIO, RMON and Register-File blocks
- Reference design with basic generator/checker synthesizable binaries
- Example design for interface to an external Marvell 88E1111 Ethernet PHY device
- Self checking behavioral models and test benches for simulation (encrypted/obfuscated)
- Design guide(s) and user manuals

Contact and Sales Information

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MAC Resource Utilization

The MAC core contains two configurable depth FIFOs on both TX and RX user interfaces, for frame buffering. The following table provides the resource utilization for the Tri-MAC with 1KB FIFO depths.

The Tri-MAC core has been fully verified on different hardware platforms for both Altera and Xilinx FPGAs.

Tri-MAC - Resource Usage for Xilinx Devices

Device	Slice LUTS	Slice Registers	BRAMs
UltraScale/ Ultrascale+	1,909	2,157	*18K = 1; 36K = 1*
7-Series	1,950	2,156	*18K = 1; 36K = 1*

Tri-MAC - Resource Usage for Altera Devices

Device	Combinational ALUTS	Registers	Memory (M20K)
Arria 10	1,561	1,846	2
Stratix V	1,565	1,814	2