A Modular and Power-Intelligent Architecture for Wireless Sensor Nodes

David Riley and Mohamed Younis
Dept. of Computer Science and Electrical Engineering
University of Maryland Baltimore County
Baltimore, MD 21250
{d17, younis}@umbc.edu

Abstract—**The current state of the art in wireless sensor nodes, both in academia and industry, is a fractured landscape of designs mostly addressing individual problems. The most common commercial design derives directly from a mote developed at the University of California, Berkeley around 1999, and presents only moderate, incremental improvements over the original design. No designs yet present a comprehensive, intelligent solution befitting a modern system. By using dynamic power management, deep system configurability, autonomous peripheral modules, and multiple CPU architectures, this paper presents a flexible and efficient node architecture. Modules on a sensor node communicate with each other to coordinate their activities and power levels. Special attention is given to power sourcing and distribution. The platform may be configured to efficiently work with most networks, sensor types and power sources due to its improved connectivity and hierarchical design. The resulting Configurable Sensor Node (CoSeN) architecture is competitive with existing designs on price, size and power while greatly exceeding most of them on performance, configurability and application potential. CoSeN is validated through prototype implementation.**

Keywords: **Wireless Sensor Node, Power Management, Modular and Configurable Design.**

I. Introduction

Recent years have seen growing interest in the applications of wireless sensor networks (WSNs) [1][2]. Examples of these applications include battlefield surveillance, security and disaster management, habitat monitoring, factory safety assessment, hazard detection in urban areas, etc. A WSN is composed of a number of sensor nodes that autonomously operate in attended setups. Data gathered from multiple sensors are processed to monitor events in an area of interest. Nodes in a WSN establish wireless links and collaborate with each other to execute application tasks. A sensor node is usually battery-powered and combines sensing, computation and communication capabilities in a small form factor. In addition to the sensing circuitry, a typical sensor node includes a microcontroller, memory and a radio.

Many WSN applications serve in inhospitable environments where nodes cannot be accessed to replace their batteries when they become depleted. Energy is thus a scarce resource for sensor systems and must be managed to extend the life of nodes for the duration of their mission. Extending battery life is also important from operational cost and convenience points of view, even for applications in which sensor nodes are accessible and maintainable. Contemporary designs for WSNs pursue energy optimization at various layers of the communication protocol stack [4] by employing low-power electronics, power-down modes, and efficient modulation [3], and through selective activation of nodes [5].

Despite extensive research on the management and operational aspects of WSNs, little attention has been paid to the design of the sensor node itself. While a number of different basic designs exist, few provide clearly discernible advantages [6][7][8]. Most current successful designs are simply iterations in design of a mote developed at the University of California, Berkeley around 1999 [6]. Existing node architectures provide little flexibility and configurability. Daughter boards may provide sensing capabilities, but the processing and communication modules are fixed and cannot be extended. This limitation constrains the usability of a design across various applications. Furthermore, power management is only possible at a macro level with little support for fine-grained and aggressive power conservation measures.

This paper presents a novel architecture for wireless sensor nodes that fills the current technology gap. The Configurable Sensor Node (CoSeN) architecture enables deep customization and assembly of a node using basic modules. A node may have many processing and sensing modules. Various configurations can be made easily, much like attaching Lego blocks. CoSeN strives for the lowest power consumption possible by dividing processing tasks along logical boundaries in order to use the most appropriate devices for each task and maximize the sleep time of each component. It also supplies a cornucopia of connections on the interconnect bus between host and peripheral boards, allowing a high degree of expandability and flexibility to meet application specific requirements. Multiple power rails, including a regulated one with dynamic voltage scaling, are provided in order to enable fine-grained energy management. A prototype implementation has confirmed the feasibility of the concept and demonstrated its superior power usage profile.

This paper is organized as follows. The next section discusses related work. Section III describes the new sensor node design in detail. In Section IV, we report on a prototype-based validation of the proposed architecture. Finally, section V gives a summary and describes on-going and future work.

II. Related Work

A large body of work exists on the design and implementation of early sensor nodes [10][11]. The design criteria for these

early nodes were loosely defined, as the field of networked sensors was still quite new. Additionally, low-power microcontrollers with sufficient computational power were scarce at the time; many early designs were necessarily constrained by the availability of hardware. Newer iterations of the design are mostly incremental improvements over the Mica mote [12][13]. Since the early motes, many different architectures have arisen, with varying degrees of success. Berkeley's Epic mote [6] attempts to reinvent the modular sensor node as a drop-in system module, while Carnegie Mellon's Firefly [7] adds determinism to the system through hardware-based time synchronization. The Libelium Waspmote provides many individual sockets for connecting off-the-shelf devices to a node [14].

Perhaps the most ambitious new node design is the Intel Mote [8], which offers a bus with advanced connection options. The second revision of the Intel Mote architecture saw a massive change in scale and scope while retaining the same sensor board interfaces [15]. The second Intel Mote provided dynamic voltage scaling capability, though only for the CPU.

All these designs have made either incremental improvements without major enhancements in expandability, modularity and fine-grained power management, or they have targeted individual problems without a comprehensive solution.

III. CoSeN Architecture

The CoSeN architecture is a highly modular approach to system design. It aims to create highly configurable nodes by clearly separating tasks along logical boundaries while providing a high degree of connectivity between the various components. An advanced, multi-rail power system with fine-grained dynamic voltage scaling serves to lower the overall system power consumption while accommodating a wide variety of devices. In this section we present an overview of the salient features of the CoSeN architecture, followed by more in-depth discussion of the design and the important aspects of the system.

A. Requirements and Desired Features

WSNs typically require specific attributes from their nodes. In general, the nodes need to be small and low-power. Nodes should also be very modular in order to handle a variety of applications. The following are the key requirements and features for sensor nodes that CoSeN opts to achieve:

Low Power Consumption: Power consumption is a significant concern for WSNs. A power consumption comparison between designs is often done on the basis of the power drawn in sleep and active modes, since most nodes will spend large amounts of their time asleep. Active consumption with radio-equipped nodes is frequently specified as the radio's power consumption, since the radio often consumes much more power than the CPU. Occasionally, CPU-only active power is also specified. The current state of the art consumes about 8 µA sleep power and 16-17 mA active radio power. A new node should not significantly exceed these consumption levels without good reason.

Modularity and Configurability: It is challenging and often counterproductive to design a single sensor node to fulfill all or most potential roles. A robust design should use a number of standard interfaces in order to connect to modules which provide features necessary for the application. Simple methods for adaptation to other standards should also be provided. A highly configurable system should also not lock the user into a single communications medium or CPU architecture.

Fine-grained power Management: Dynamic voltage scaling is highly desirable for sensor node platforms. It can be challenging in expandable systems where unknown modules may be attached, but an intelligent platform can manage voltage level changes upon request while ensuring that no components are damaged by overvoltage. The system should be able to run at the lowest possible voltage most of the time while still providing for parts which require (or perform better at) higher voltages.

Autonomous Peripherals: Many modern microcontrollers have extremely low sleep power consumption, often only a few hundred nanoamps. There is little reason that peripheral modules should not have autonomous control processors to manage their components. This allows the main CPU, which may be fairly power-hungry in some implementations, to sleep while the peripheral module goes about its own business of sensing, communicating, etc. The peripheral board can wake the CPU when it has a significant amount of data available to transfer, reducing CPU interrupt overhead.

Support of Multiple CPU Architectures: Most existing sensor node platforms focus exclusively on one CPU architecture. For example, the Berkeley motes have until recently focused almost entirely on the AVR architecture. Supporting multiple CPU architectures gives the user flexibility to choose the most appropriate CPU platform for their application.

B. Detailed Design

The CoSeN architecture defines a next-generation sensor node platform. CoSeN is a hierarchical design with defined roles for its major components. A block diagram of a sample system is shown in Figure 1. A system is composed of one baseboard and one or multiple peripheral boards that augment the node with application specific functionality. However, unlike prior work pursue similar approach, the expansion scheme provides both autonomy to the peripheral boards and enable cross-module power optimization and sharing of proposing load. The functional components are described below.

Processing Components: The processing is divided into three roles. The Central Processing Unit (CPU) handles application-specific tasks; the Host Management Controller (HMC) coordinates system-wide activities; and the Module Management Controllers (MMCs) on each peripheral board manage the local tasks of their boards. Peripheral devices are connected to the system through standard protocols such as I^2C and SPI buses as well as analog lines. A set of interrupt lines

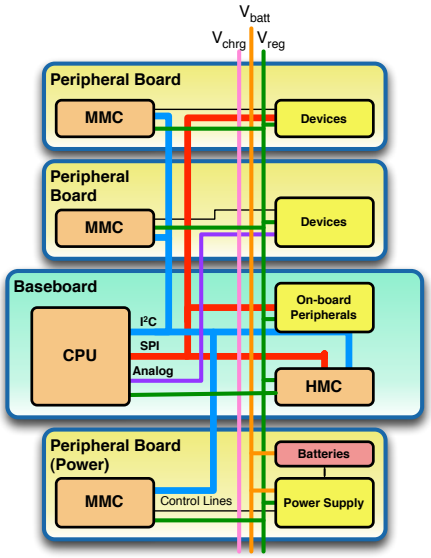

Figure 1: CoSeN system conceptual block diagram

(not shown in Figure 1) allows peripherals to wake the CPU to perform tasks such as data transfer. The baseboard may also include peripherals to reduce the system size.

Power Consumption and Management: The CoSeN architecture implements advanced power management methods to achieve low power consumption and improve modularity. Power is reduced by providing a dynamically scalable regulated voltage power rail, while modularity is improved by providing raw battery and charging power rails.

Dynamic voltage scaling is used to reduce system power consumption while preserving performance levels. The system runs at the lowest possible voltage most of the time. Peripheral boards are allowed to temporarily raise system voltage to a desired level while performing their tasks. CoSeN provides dynamically scalable voltage via a regulated power rail (V_{reg}), which functions as the main supply rail for the system. System components collaborate to establish the operating voltage at run-time. The HMC tracks individual device voltage limits to prevent inadvertent device damage due to overvoltage.

The system provides three power rails to devices; the aforementioned V_{reg}, battery voltage V_{batt}, and optional charging voltage V_{chrg}. V_{reg} is typically derived from V_{batt} by a voltage regulator; individual sub-systems may use V_{batt} to monitor battery health, derive their own local voltages, or even charge their batteries using higher voltages from V_{chrg}. Any module in the system may source or sink any rail; this permits modules such as independent power supply and energy harvesting boards to be used.

Connectivity and Mechanical Form Factor: A CoSeN module is miniaturized, but its size may diminish as technology advances. Based on today's technology, its 1.5 inches square size was easily achieved in a prototype implementation (as discussed later in the paper). Devices which require protrusions, e.g., for antennae or cable connections, may exceed these dimensions as necessary. The modules of a CoSeN system stack vertically using a high-density, 80-pin locking connector in order to provide sufficient rigidity for most applications and support device mobility and high vibration in for particularly high-stress environments.

CoSeN's high pin count connector provides inter-module interfaces for power, address, data and control. CoSeN also calls for priority-based interrupt lines, a global line for an RTC clock pulse, and dedicated debugging pins for application development. Standard interfaces for peripheral modules are provided. Examples include SPI, I^2C, and UART buses. For instance, processors in a system connect to each other through I^2C and the host transfers high-speed data via SPI.

Modularity and Autonomous Peripherals: Each peripheral module has an on-board microcontroller (the Module Management Controller, or MMC) which manages its functionality and identifies it to the system. The MMC is responsible for handling peripheral board activities such as sampling or network communications while the CPU sleeps or performs other application-specific tasks. This improves power consumption by decreasing the interrupt overhead of the CPU (and potentially its sleep time). It also improves system modularity by insulating the low-level function of devices from the CPU, which may then communicate with standard peripheral classes via simplified standard interfaces.

Peripheral activities, including requests for voltage changes, are coordinated by the HMC, which resides on the baseboard with the CPU. The HMC's job, aside from acting as MMC for peripherals integrated on the baseboard, is coordinating system activities such as resource assignment at boot time and dynamic voltage changes at run time. The HMC may be a CPU task in some implementations, or it may be a separate processor on the baseboard. Peripheral boards are not constrained to be simply sensor boards. They may contain power supplies, storage, communications interfaces such as Ethernet or 802.11, or even interfaces to attach to other systems such as robots. Anything that cannot be directly attached to the bus can be adapted through the board's MMC.

Communications are implemented through the MMCs on peripheral boards (or the HMC, if the communication peripheral is on the baseboard). The CPU communicates with the MMC using a generalized networking approach based on the Berkely sockets system, while the MMC handles low-level protocol tasks such as media access and packet handling. Medium-specific tasks, such as joining or discovering link quality, are provided as extensions to the basic protocol.

IV. Approach Validation

A prototype baseboard for the CoSeN system has been built to test system concepts under real-world conditions. The prototype implements a highly integrated baseboard consisting of an 8-bit CPU, a 2.4 GHz radio, non-volatile storage and a power supply. Initial tests indicate good power results at standard battery voltages.

A. Implementation Details

The prototype board uses an Atmel ATXMEGA32A4 microcontroller as its CPU and HMC. This CPU was chosen for its I/O features and low power as well as the availability of

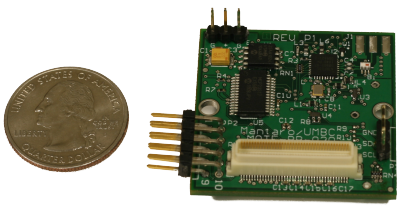

Figure 2: CoSeN prototype device, with quarter for size reference

open-source tools with which to develop code for it. The CPU is similar to the ATMEGA CPUs used in many wireless sensor nodes. RF functionality is provided by an Atmel AT86RF231, with a reverse-polarity SMA connector for an antenna. This is the lowest-power IEEE 802.15.4 IC currently available. It also includes advanced features beneficial to low-power wireless systems, such as extended data rates and additional communications offload to extend CPU sleep time.

A Linear LTC3388 switching power supply IC provides regulated power on V_{reg}. This regulator is the only switching regulator currently on the market with acceptable efficiency (>80%) for currents typical of low-power sensor nodes.

B. Preliminary Experimental Results

The prototypes were tested to evaluate the power consumption of the modules in various operating modes. The boards were run with a set of test software designed to exercise various sleep and run modes on both the CPU and the RF IC. A bench power supply was used to supply V_{batt} at voltage levels close to those likely to be seen in the field. Power was supplied at voltage levels of 2.7, 3.0 and 5.0 volts. The 3.0 and 2.7 volts correspond to the ordinary start- and end-of-life voltages for a lithium coin cell, respectively, while 5.0 volts represents an approximate maximum likely voltage to be seen in the field. Measurements were performed with a Fluke 87V multimeter. All measurements averaged for 15 minutes each.

Mode	V_{batt} = 2.7v	V_{batt} = 3.0v	V_{batt} = 5.0v
Power Down	1.7µA	1.35µA	1.307µA
Power Save (with RTC)	3.0µA	3.6µA	2.0µA
Idle (2 MHz)	273.9µA	297µA	135µA
Run (2 MHz)	637.8µA	728µA	368µA
Radio Rx (no signal)	10.01mA	8.89mA	5.84mA
Radio Tx (+3dBm)	11.50mA	10.40mA	6.75mA

Table 1: Power measurements for the CoSeN prototype.

The power measurements are shown in Table 1. The comparison to competing nodes is stark. The most recent entries in the Berkeley Mote family (Memsic's Iris and Lotus motes) both claim sleep currents of 8 µA and radio active currents of 16 and 17 mA for receive and transmit, respectively at battery voltages of 2.7-3.3 volts. Our results are nearly 50% better for active mode. Some measurements at 3.0v indicate anomalously higher currents than 2.7v, which requires further investigation of the measurement strategy.

V. CONCLUSION

In this paper, we have presented CoSeN, a new wireless sensor node architecture with unprecedented configurability and power management capabilities. CoSeN reduces power consumption using dynamic power management and autonomous peripheral modules, and produces a highly configurable system by providing high connectivity using standard protocols with automatic resource distribution. We have also demonstrated the feasibility of the platform through a prototype which outperforms current sensor node platforms on power consumption by a factor of nearly 50%.

Additional work is needed to establish the CoSeN architecture's place in the wireless sensor network ecosystem. Peripheral boards, including sensors, storage and other communication interfaces, are being developed to further test the ability of the platform to self-configure and sample real-world data. Baseboards with different CPUs, such as MSP430 and ARMs, are under evaluation to test power and space efficiency of other architectures. A large network must be constructed to test the prototype's RF performance under strain. Finally, a complete software stack must be released in order to build a community to develop the architecture.

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