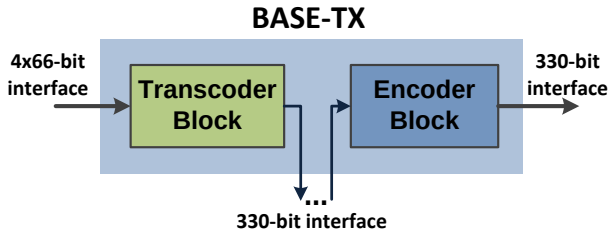
Reed-Solomon FEC IP Solution

Product Brief (HTK-RS-FEC-FPGA)

The Reed-Solomon Forward Error Correction (RS-FEC) IP Solution implements the RS-FEC sublayer specified in IEEE 802.3by/D3.1. This high through-put design is targeted for demanding, high frequency applications and provides bypass capabilities for direct access to sub designs. The target frequency is **390.625MHz** for up to 100Gbps operation.

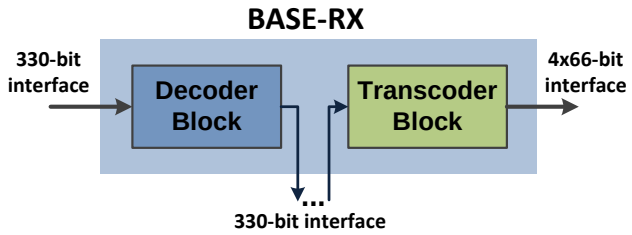
Features Overview

BASE-TX Core Features



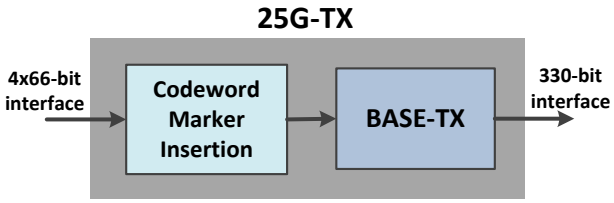
- Implements base modules for the RS-FEC transmitter which includes RS encoder, 64b/66b to 256b/257b transcoder and gearbox logic
- Implements 4x66-bit interface for 64b/66b to 256b/257b transcoder
- Implements 257-bit to 330-bit gearbox logic for interconnection between transcoder and encoder
- Implements 330-bit encoder interface for Reed-Solomon code RS(528,514,10) with polynomial specified in 802.3by specifications
- High through-put, low latency encoder processes 33 symbols in parallel
- Valid based implementation allows discontinuous data flow and/or bandwidth controlled operation
- Implements a fixed latency memory-less design with direct access to RS encoder and transcoder blocks

BASE-RX Core Features



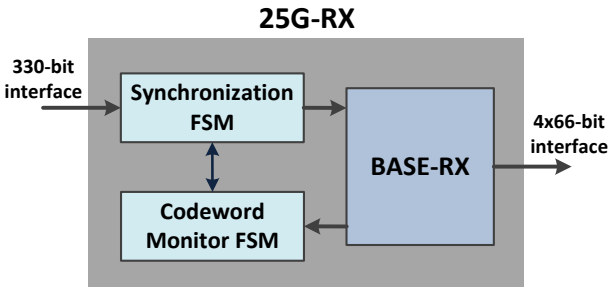
- Implements base modules for the RS-FEC receiver which includes RS decoder a, 256b/257b to 64b/66b transcoder and gearbox logic
- Implements 330-bit decoder interface for Reed-Solomon code (528,514,10) with polynomial specified in 802.3by specifications
- Implements 330-bit to 257-bit gearbox logic for interconnection between decoder and transcoder
- Implements 257-bit interface for 64b/66b to 256b/257b transcoder
- High through-put decoder processes 33 symbols in parallel
- Decoder provides detection of uncorrectable codewords and corresponding 257-bit blocks are corrupted at transcoder output as per 802.3by specifications
- Direct access to RS decoder and transcoder blocks is available

25G-TX Core Features



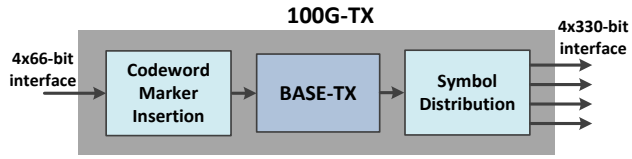
- Implements all the features of BASE-TX Core
- Supports 25G codeword marker insertion with markers specified by 802.3by specifications

25G-RX Core Features



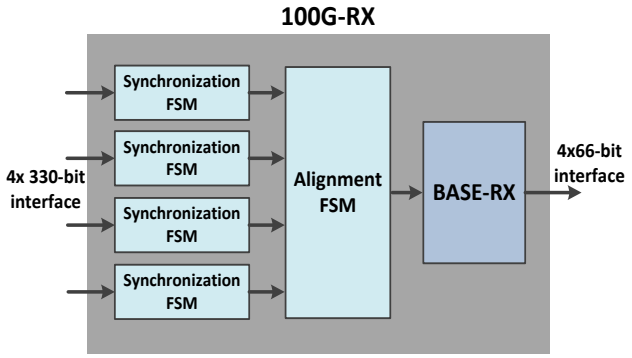
- Implements all the features of BASE-RX Core
- Implements 330-bit block synchronization state machine as specified in 802.3by specifications.
- Implements codeword monitor state machine as specified in 802.3by specifications

100G-TX Core Features



- Implements all the features of BASE-TX Core
- Supports 100G codeword marker insertion and mapping with markers specified by 802.3bj specifications
- Implements symbol distribution to four lanes as specified in 802.3bj specifications

100G-RX Core Features



- Implements all the features of BASE-RX Core
- Implements 330-bit block synchronization state machine as specified in 802.3bj specifications
- Implements alignment state machine as specified in 802.3bj specifications

Licensing and Maintenance

- ***NO yearly maintenance fees for upgrades and bug fixes***
- Basic core licensing for a single vendor (either Xilinx or Altera) compiled (synthesized netlist) binary
- Other licensing options include:
  - Vendor and device family agnostic source code (Verilog) license
  - A ***low cost, board locked*** license for low budget prototyping (upgradeable to full license)

Contact and Sales Information

For further information, contact sales representative at:

Phone: +1-301-528-2244

Email: info@mantaro.com

Resource Utilization

The utilization summary of the variations of the RS-FEC core is given in the following tables. The utilization numbers are best in class as compared to other available RS-FEC core variations with a comparable feature set.

The RS-FEC solution has been fully verified on different hardware platforms for both Altera and Xilinx FPGAs.

RS-FEC IP - Resource Usage for Xilinx Devices

Device	*Design*	*Slice LUTS*	*Slice Registers*	*BRAMs*
UltraScale/ UltraScale+	BASE-TX	8,100	5,000	*18K = 0; 36K = 0*
	BASE-RX	24,300	14,900	*18K = 0; 36K = 0*
	25G-TX	8,200	5,000	*18K = 0; 36K = 0*
	25G-RX	24,400	15,800	*18K = 0; 36K = 0*
	100G-TX	8,500	6,300	*18K = 0; 36K = 0*
	100G-RX	29,200	22,800	*18K = 0; 36K = 0*
7-Series	BASE-TX	8,100	5,000	*18K = 0; 36K = 0*
	BASE-RX	24,500	14,800	*18K = 0; 36K = 0*
	25G-TX	8,200	5,000	*18K = 0; 36K = 0*
	25G-RX	24,600	15,700	*18K = 0; 36K = 0*
	100G-TX	8,500	6,300	*18K = 0; 36K = 0*
	100G-RX	29,600	22,700	*18K = 0; 36K = 0*

*The resource utilization provided is preliminary

RS-FEC IP - Resource Usage for Altera Devices

Device	*Design*	*COMB. ALUTs*	*Registers*	*Memory M20K*
Arria 10	BASE-TX	5,700	5,000	0
	BASE-RX	21,900	18,600	0
	25G-TX	6,000	5,100	0
	25G-RX	22,000	20,200	0
	100G-TX	7,300	6,500	0
	100G-RX	24,300	25,200	0
Stratix V	BASE-TX	5,700	5,000	0
	BASE-RX	21,300	17,700	0
	25G-TX	6,000	5,200	0
	25G-RX	21,400	19,400	0
	100G-TX	7,300	6,600	0
	100G-RX	23,700	24,600	0

*The resource utilization provided is preliminary